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True-Average Current-Mode Control of DC-DC Power Converters: Analysis, Design, and Characterization

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TRUE-AVERAGE CURRENT-MODE CONTROL OF DC-DC POWER CONVERTERS: ANALYSIS, DESIGN, AND CHARACTERIZATION

A dissertation submitted in partial fulfillment

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Doctor of Philosophy

By

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I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Dalvir K. Saini ENTITLED True-Average Current-Mode Control of DC-DC Power Converters: Analysis, Design, and Characterization BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy.

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Abstract

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Energy efficient, wide-bandwidth, and well-regulated dc-dc power converters are in great demand in today's emerging technologies in areas such as medical, communication, aerospace, and automotive industries. In addition to design and selection of the converter components, a robust closed-loop modeling is very essential for reliable power-electronic systems.

Two closed-loop control techniques for power converters exist: voltage-mode control and current-mode control. The principles of voltage-mode control have been explored in great depths by researchers over the last two decades. However, the dynamic modeling of current-mode controlled dc-dc power converters has many uncharted areas that needs careful attention. Two main methods exist under the category of current-mode control: peak current-mode control and average current-mode control. Both of these control strategies are very attractive in applications that require fast control speeds, improved voltage regulation, and improved power supply noise rejection ratio. In recent technological advancements, where high noise immunity and tight regulation are desired, the average current-mode control has proven to be a superior choice, when compared to other control techniques for power converters.

In this dissertation, a complete systematic theoretical framework for analysis, design, characterization, and measurements of the dc-dc converters with average current-mode control is introduced. To overcome the drawbacks of the traditional average current-mode control method, a new "true-average" current-mode control technique is proposed. The new technique is implemented on the basic converter topologies namely, buck, boost, and buck-boost. The dynamic small-signal models of

the converter power-stages are developed using the circuit-averaging technique. The inner-current loop of the power converters is designed and their frequency-domain, time-domain, and pole-zero domain characteristics are exploited. Subsequently, the outer-voltage loop is designed in the presence of current-controlled power stage and the overall converter performance is evaluated against dynamically-varying operating conditions.

A laboratory prototype of a buck-boost converter for 12 V to 5 V at 25 W operating at 200 kHz was designed, built, and measured. The theoretically predicted results were validated both through simulations and experiments. The techniques to measure the small-signal open-loop and closed-loop transfer functions are also provided. Excellent agreement between the theoretical and experimental results were observed.

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Acknowledgments

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1 Introduction

Current-mode control of pulse-width modulated dc-dc converters has been one of the most challenging and interesting topic of study in the vast field of power electronics for almost two decades. Even to this day, rigorous research to establish a solid and a systematic characterization of current-mode controlled dc-dc power converters is being performed. Current works in current-mode control are focused towards the analysis, design, modeling, and its efficient implementation in a wide-variety of important applications such as power factor correctors, battery chargers, and LED drivers. This dissertation aims to develop a complete characterization of average current-mode controlled basic dc-dc power converter topologies.

Current-mode control, particularly *peak current-mode control* was invented by Cecil W. Deisch of Bell Labs/Western Electric in 1978 [1]. The invention mainly helped to balance the ac flux in a transformer of a push-pull converter in order to keep the core from walking off into saturation caused by a minor difference in the volt-sec balance, which generally occurred in converters with slightly asymmetric drive waveforms or due to load transients. In view of the growing demand for dc-dc converters, especially in military, telecommunication, and aerospace industries, it became extremely necessary to develop static and dynamic models of power electronic systems. Dr. Slobodan Ćuk first introduced the state-space averaging technique, where the circuit behavior in switching sub-intervals were mathematical represented in the form of state variables- with the state variables being the inductor current or capacitor voltage. Pioneer research, which realized the important aspects of closed-loop stability of peak current-mode controlled dc-dc converters was conducted by Dr. David Middlebrook and Dr. F. D. Tan of California Institute of Technology in 1985. These works even to this day serve as a starting point for establishing stability criteria, especially in cascaded or multi-level power converters [2]-[5].

The concept of average current-mode control was re-instated by Lloyd Dixon from Unitrode Electronics in 1990 [9], [10]. In the following years, closed-loop modeling of average current-mode controlled ac-dc and dc-dc converters were performed by various researchers including Raymond B. Ridley [6]-[8] and Jian Sun *et al* [27].

Before describing the principle of operation of average current-mode control, it is imperative to discuss properties of peak current-mode control. Fig. 1.1 shows the basic circuit of a peak current-mode controlled boost dc-dc converter. In peak current-mode control, the peak of the inductor current waveform is tracked and controlled. The peak inductor current is compared to the current reference (or current program) set by the outer voltage loop of the dc-dc converter. As the peak value of the sensed inductor current becomes equal to the current reference, the comparator outputs a logic high at the instant of comparison and is logic low for all other values. The comparator output is connected to the reset pin of the RS-latch, whereas the set pin is connected to a clock tuned to operate at the switching frequency. Initially, the set pin enables the latch output to switch ON state. Eventually, as the reset pin receives a logic high, the output of latch resets the switch to OFF position and remains in this state until the clock sets it back to high position. The following demerits are observed as a consequence of the operation of peak current-mode control:

- Highly susceptible to noise- At the instant of comparison of the peak inductor current and the current reference, a noise spike is created. The noise signal can create false triggering of the logic gates resulting in undesirable switching events.

- Slope compensation required- The peak current-mode control needs slope compensation circuitry for duty ratio higher than 0.5 in order to avoid instability. The fixed compensation ramp provides adequate compensation, however will overcompensate much of the time, resulting in performance degradation and

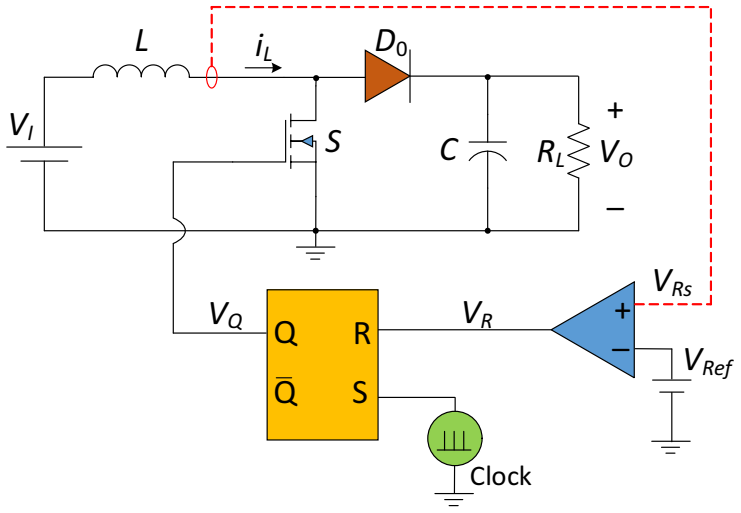

Figure 1.1: Basic circuit of a peak current-mode controlled boost dc-dc converter.

increased distortion [9].

- High peak to average current ratio- The inductor current peak to average ratio is high. Therefore, the outer voltage loop cannot completely eliminate this error between the peak and the average values. This is a problem, especially in power factor corrector converters and causes distortion in the input current waveform.

- Uncompensated current loop gain is low- In the classical peak current-mode control, the uncompensated loop gain is very low. Therefore, stronger compensation schemes such as Type-II and Type-III voltage error amplifiers are needed to boost the loop gain at dc.

1.1 Principle of Operation of Existing Average Current-Mode Control Technique

In the conventional average current-mode control, the time-varying average value of the sensed inductor current is regulated. Fig. 1.2 shows the circuit of a buck dc-dc converter with the conventional average current-mode control scheme. The reference to the current loop is set by the outer loop. The current reference generated by

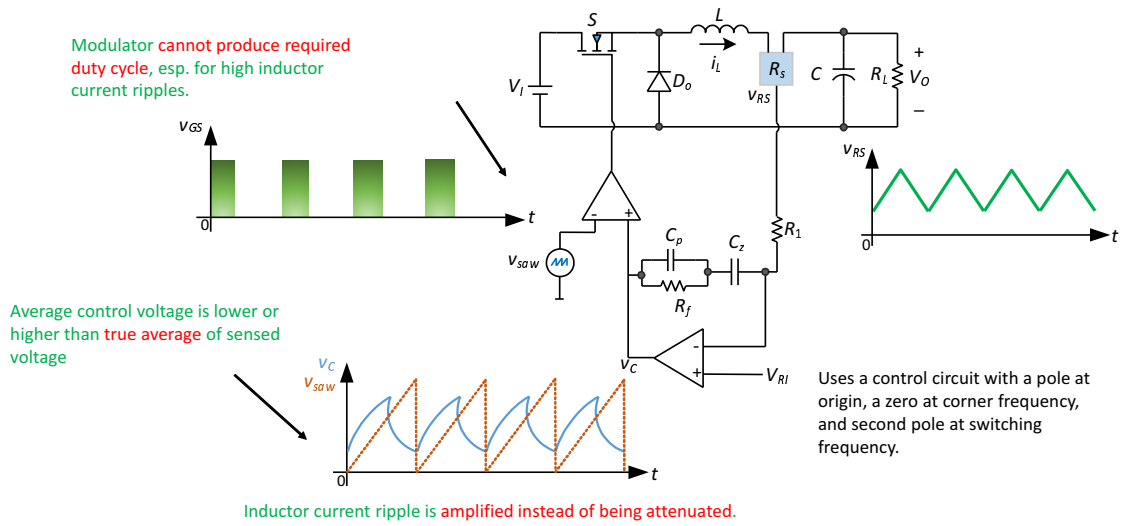

Figure 1.2: Circuit of a buck dc-dc converter with the conventional average current-mode control scheme [9].

the outer voltage loop is set to be equal to the desired inductor current average. A high gain integrating amplifier in the current loop attempts the track the average value of the inductor current and outputs the amplified current error to a pulse-width modulator. The amplified current error is compared to a large amplitude sawtooth waveform oscillating at the switching frequency at the PWM comparator inputs.

Unlike in peak current-mode control, the current loop gain can be modified for optimum performance by the compensation network in the current loop. For example, it is possible to have equal loop gain crossover frequencies in both peak current-mode and average current-mode control schemes, but the gain will be much greater in average current-mode control at lower frequencies. This is essential to reduce the steady-state error significantly.

Although, the conventional average current-mode control has unique advantages over peak current-mode, a few challenges were encountered. Fig. 1.3 shows the duty cycle, sensed inductor current v_{RS}, output of current error amplifier v_{Ci}, sawtooth waveform v_{saw}, and gate-to-source voltage waveform relevant to a buck dc-dc con-

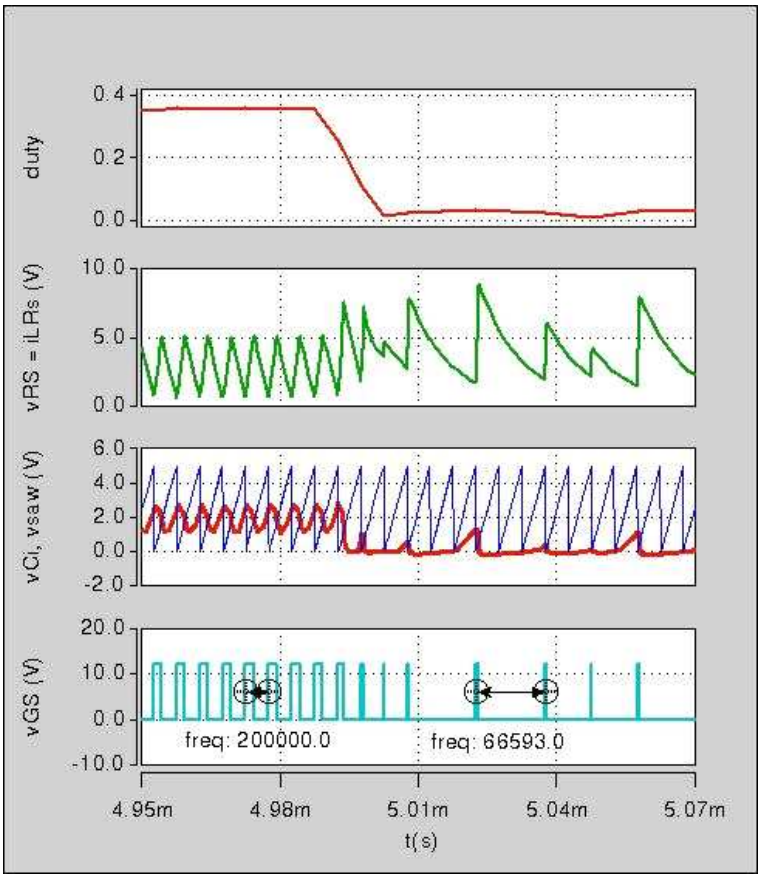

Figure 1.3: Waveforms showing the challenges encountered with Dixon's method of average current-mode control.

verter. As the input voltage increases, the duty cycle must reduce. At low duty cycles, the inductor current ripple increases in magnitude. Since the error amplifier, basically magnifies the error between the sensed inductor current and the current reference, the large inductor current ripple is also amplified . Therefore, the comparison between the sawtooth waveform and the amplified error output takes place more than once in each switching period resulting in subharmonic oscillations. This drawback cannot be ignored especially in converters used as power factor correctors. Also, this method limits the designer from implementing switch current sensing due to larger current magnitudes. Moreover, even under normal operating conditions, the current-loop error amplifier must filter the switching frequency component in

the sensed inductor current as well as perform normal compensation functions. In this technique, the inductor current is sensed and converted into sensed voltage by a current-to-voltage transducer. The sensed voltage comprises of both dc and switching frequency ripple and is supplied to the control circuit. An integral single-lead (or Type II) control circuit is used in this technique, which performs two tasks:

1. Provides the required compensation for the inner loop.

2. Acts as a low-pass filter to reduce the switching frequency ripple in the sensed voltage. The control circuit comprises of a pole at origin and a single pole-zero pair located at high frequencies. The pole at the origin provides a high dc gain to reduce the steady-state error, the high-frequency zero extends the current loop crossover frequency, and the high-frequency pole must filter the switching frequency ripple in the sensed signal [27].

A few evident shortcomings of this technique are as follows:

- The control circuit has a limited degree of freedom. For example, tuning its components for a desired phase margin will compromise the low-pass filter requirements and *vice versa*.

- At a high input voltage, the duty cycle is low and the inductor current ripple is high. This yields a large ripple at the control voltage supplied to the pulse-width modulator. The slope of the control voltage exceeds the slope of the carrier voltage, causing switching instability [12], [9], [27].

- Due to the above two drawbacks, pulsating or discontinuous currents such as the switch current or diode current in the converter cannot be effectively sensed.

- Since the inductor current is sampled per switching period, the need for including the sampling gain becomes evident.

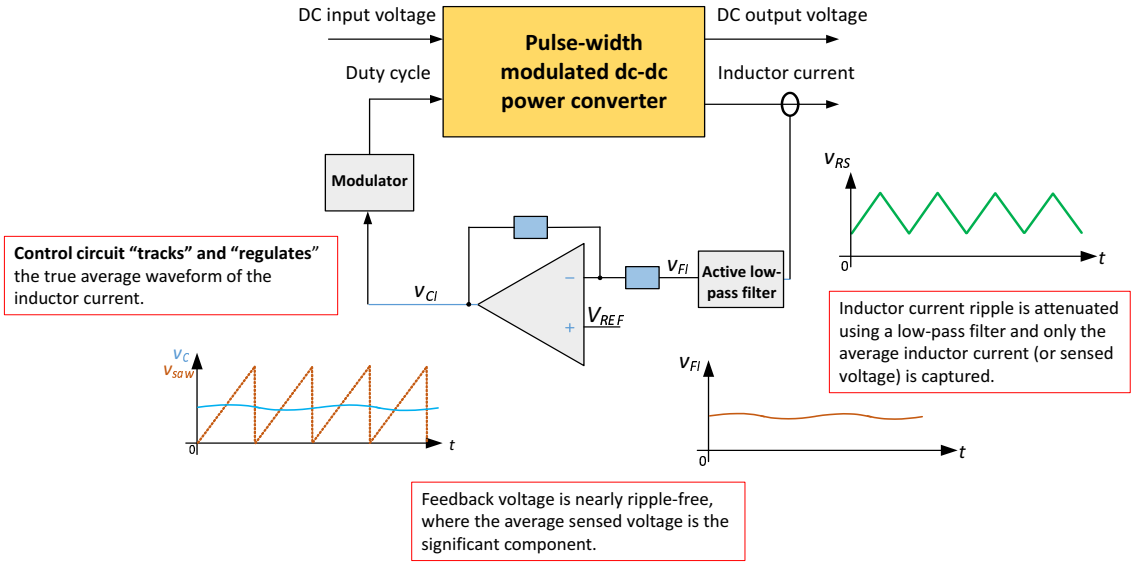

Figure 1.4: Block diagram of true-average current-mode controlled dc-dc power converters.

- The location of the high-frequency pole is close to the switching frequency. Therefore, its contribution in reducing the switching frequency ripple and proving any compensation for the inner loop at high frequencies is undermined.

Therefore, a modified circuit shown in Fig. 1.4 is proposed in this work. Here, the compensation circuit and the low-pass filter are decoupled and they function independently. The sensed voltage due to the inductor current is provided to a low-pass filter dedicated only to cancel its switching frequency component. The output voltage of the low-pass filter with a reduced switching frequency ripple component is provided to the control circuit. Thus, the control voltage also exhibits a reduced ripple.

1.2 Principle of Operation of True-Average Current-Mode Control Technique

Fig. 1.4 shows the block diagram of the true-average current-mode controlled dc-dc converter. Fig. 1.5 shows the key waveforms related to the sensing and feedback

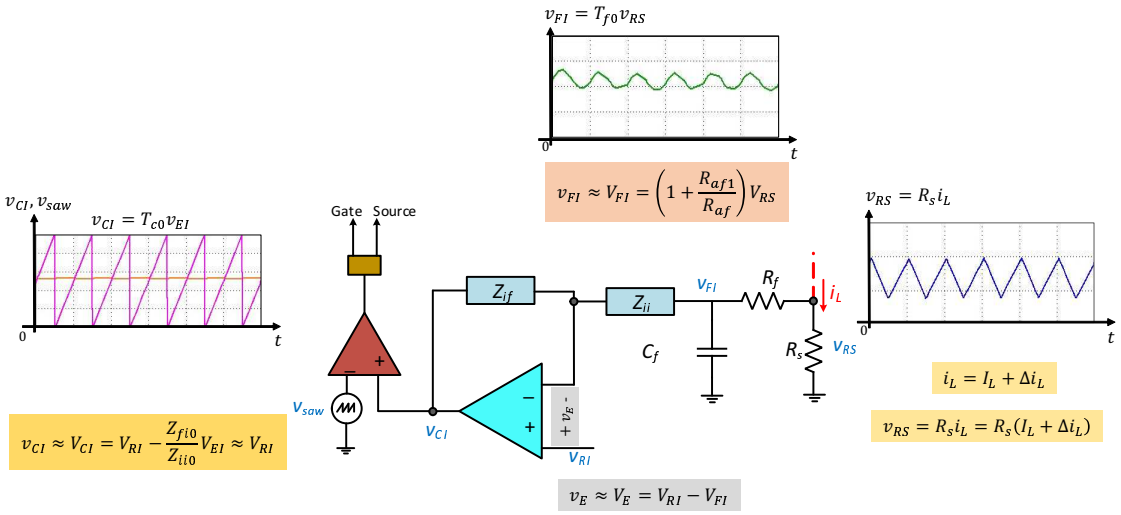

Figure 1.5: Key waveforms related to the feedback path in true-average current-mode control.

path. The sense resistor or current sensor is placed in the inductor branch to sense the inductor current. The sensed voltage is v_{RS}. The sensed voltage is provided to an low-pass filter composed of a resistor and capacitor network. The switching frequency component is eliminated by the low-pass filter, therefore, the filter output voltage is dc with negligible ripple. The effective feedback voltage to the inner loop is v_{FI}. The reference voltage to the inner current loop v_{RI} is governed by the outer voltage loop. Based on the desired parameters such as high bandwidth and high dc gain of the inner current loop, an appropriate control circuit with forward path impedance Z_{ii} and the feedback path impedance Z_{fi} will be derived and is a topic of discussion in the subsequent sections. The control voltage v_{CI} at the output of the controller is compared with a sawtooth waveform v_{saw}, which generates the duty cycle d_T. By virtue of circuit operation, the true average value of the inductor current (or any branch current) is sensed and controlled by the inner current loop.

The major advantages of using the modified technique are :

1. The compensation and filtering processes are performed independently. A good selection of the filter cutoff frequency assists the dynamic response and will be

shown further.

2. The feedback voltage to the control circuit contains primarily the average value of the sensed current and the switching frequency component is negligible. Therefore, a discontinuous switch or diode current with large amplitudes, a continuous or discontinuous inductor current of any amplitude, or the load current can be sensed by placing the current sensor in the corresponding branch.

3. The low-pass filter can be placed either in the feedback path or the forward path to reduce the ripple in the control voltage.

4. Due to the presence of the low-pass filter, the current loop does not behave as a sampling system. Thus, the effect of sampling gain is eliminated.

5. The problems due to switching instability are completely avoided as the control voltage intersects the carrier voltage only once during each switching period.

While the circuits addressed in [13]-[16] use the modified average current control scheme for buck and cascaded boost converter topologies, their tuning procedure and their inner loop analysis has not been reported. This work endeavors to present a complete inner loop analysis of different power converters, whose average inductor current is regulated by the proposed modified current-mode control scheme. The steady-state large-signal operation, open- and closed-loop transfer functions, and transient characteristics are presented.

1.3 Steady-State Operation

The inductor current comprises of switching frequency component Δi_L superimposed on dc value I_L. The potential difference across the sensed resistor R_S is given as

$$v_{RS} = R_s i_L = R_s(I_L + \Delta i_L). \tag{1.1}$$

The filter eliminates the switching frequency component of v_{RS}. By selecting appropriate sense resistance R_s, V_{RS} can be made equal to V_{RI}, where V_{RI} is the current reference voltage. The output voltage of the active filter is then compared to the reference voltage V_{RI}. The error signal is given as

$$V_{EI} = V_{RI} - V_{FI}. \tag{1.2}$$

The error signal is the input to the controller. The output of the controller is given as

$$V_{CI} = V_{RI} + T_{ci0} V_{EI}, \tag{1.3}$$

where T_{ci0} is the dc gain of the controller. The pulse-width-modulator circuit is an inverting op-amp comparator. The control voltage is applied to the non-inverting input and the sawtooth voltage signal v_{saw} is applied to the inverting input of the comparator. For any change in the control voltage v_C from V_C to $V_C + v_c$, the duty cycle d_T also changes from D to $D + d$. The control voltage-to-duty cycle transfer function of the pulse-width modulator is expressed as

$$T_m = \frac{D}{V_{CI}} = \frac{1}{V_{Tm}}, \tag{1.4}$$

where V_{Tm} is the amplitude of the sawtooth waveform. In steady state $V_{EI} \approx 0$, which yields $V_{CI} = V_{RI}$. From (1.4), $V_{CI} = DV_{Tm}$.

A buck dc-dc converter with the true-average current-mode control was simulated and its waveforms are shown in Fig. 1.6. Fig. 1.3 shows the duty cycle, sensed inductor current v_{RS}, output of current error amplifier v_{CI}, sawtooth waveform v_{saw}, and gate-to-source voltage waveform relevant to a buck dc-dc converter. It can be seen that as the duty cycle decreases, the inductor current ripple increases. The comparator is able to track the amplified error voltage and produce gate-to-source voltage oscillating at the switching frequency.

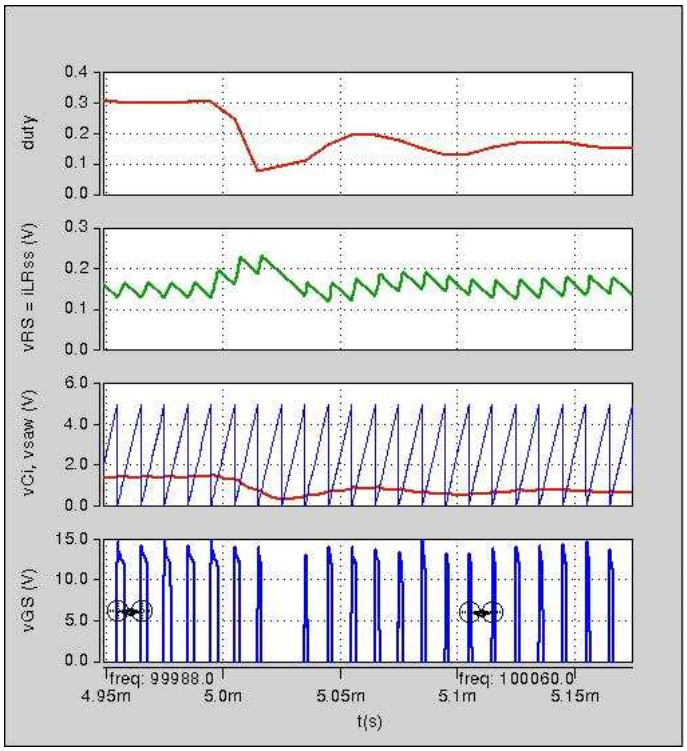

Figure 1.6: Waveforms related to the proposed true average current-mode controlled dc-dc power converters as opposed to the Dixon's method shown in Fig. 1.2.

1.4 Motivation

A systematic characterization of the true-average current-mode control (ACMC) of dc-dc converters was an open topic. The dynamic behavior, detailed design, network transfer functions, network impedances of ACMC dc-dc converters are still not reported in its entirety. The main motivations of this dissertation includes:

- To perform pioneer research related to the improvisation of existing average current-mode control theory.
- To combine the technical concepts in control theory and power conversion for the development of a *good* power supply.
- To lay the theoretical and analytical framework for future studies in this field by producing a systematic study of the dc-dc converter's static and dynamic

behavior.

1.5 Dissertation Objectives

- To identify the critical problems and challenges in the existing average current-mode control technique, for example, the Dixon's method.
- To propose the "true-average" current-mode control technique, which can potentially overcome the problems in the existing technique.
- To implement the proposed control technique on a buck-boost, buck, and boost dc-dc converters.
- To analyze the steady-state waveforms and to design the inner-current loop.
- To develop small-signal models of the inner-current loop for the buck-boost, buck, and boost converters in continuous-conduction mode.
- To derive transfer functions related to inner-current loop.
- To derive voltage-loop relevant transfer functions for the current-controlled dc-dc converters.
- To evaluate ac and transient characteristics for above-mentioned dc-dc converters.
- To verify the derived models through simulations for the two-loop system.
- To perform experimental validation for closed-loop buck-boost converter with true average current-mode control.

2 True-Average Current-Mode-Control of Buck-Boost DC-DC Converter

The circuit of pulse-width modulated (PWM) DC-DC buck-boost converter is shown in Fig. 2.1. The operation of buck-boost converter in continuous-conduction mode (CCM) is given in details in [34]. The circuit of buck-boost converter consists of a power MOSFET S, a diode D_0, an inductor L, a filter capacitor C, and a load resistor R_L. The switch is turned ON and OFF at a switching frequency f_s and at a duty cycle D. The converter efficiency is η. The aims of this chapter are:

1. To describe dc characteristics.
2. To introduce small-signal linear model.
3. To derive and analyze the open-loop power stage transfer functions.
4. To derive and analyze the open-loop input and output impedances.
5. To design and analyze a compensator circuit.
6. To derive and analyze the closed inner-current loop transfer functions.
7. To demonstrate the behavior of true-average current-mode control.
8. To derive and analyze the closed inner-current loop transfer functions.
9. To derive and analyze the closed outer-voltage loop transfer functions.

2.1 DC Characteristics

The dc voltage transfer functions of buck-boost converter for CCM are given in details in [34]. The idealized current and voltage waveforms of the switching network of

buck-boost converter is shown in Fig. 2.2. Circuit averaging technique is applied to switching network waveforms. The dc component of the switch current is

$$I_S = \frac{1}{T}\int_0^T i_s dt = \frac{1}{DT}\int_0^T I_L dt = DI_L. \tag{2.1}$$

Hence, the MOSFET can be replaced by an ideal dc current-dependent current source. The dc component of diode voltage is

$$V_D = \frac{1}{T}\int_0^T v_d dt = \frac{1}{DT}\int_0^T (V_I - V_O) dt = D(V_I - V_O). \tag{2.2}$$

The diode can be replaced by an ideal dc voltage-dependent voltage source. The dc component of the input current is

$$I_I = D(I_I + I_O) \tag{2.3}$$

and the dc component of output current is

$$I_O = (1 - D)(I_I + I_O). \tag{2.4}$$

The dc voltage transfer function of the buck-boost converter is

$$M_{VDC} = \frac{V_O}{V_I} = \frac{D}{(1 - D)} \tag{2.5}$$

and the dc current transfer function of the buck-boost converter is

$$M_{IDC} = \frac{1}{M_{VDC}}\frac{I_O}{I_I} = \frac{1 - D}{D}. \tag{2.6}$$

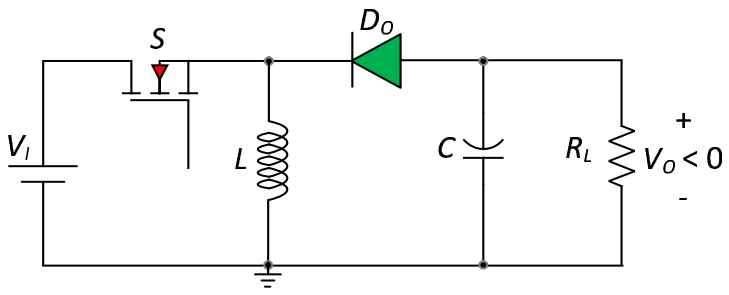

Figure 2.1: Circuit of the pulse-width modulated buck-boost dc-dc converter.

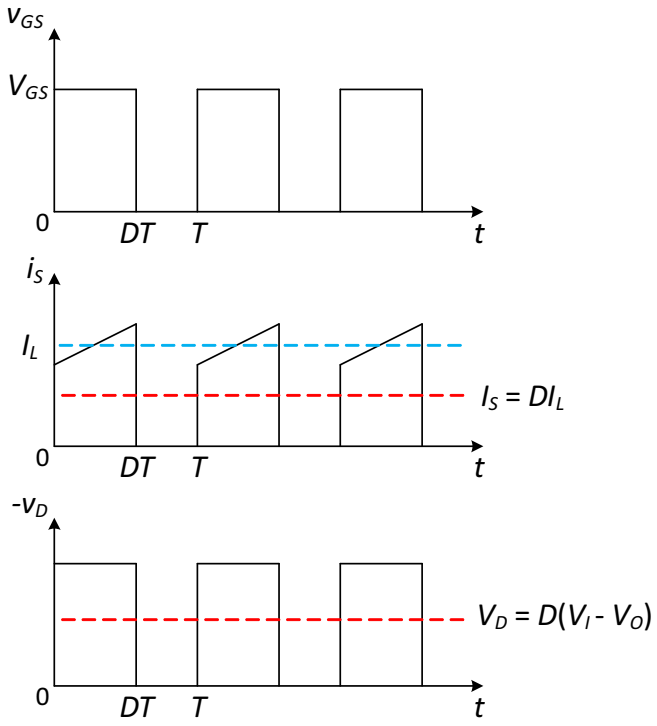

Figure 2.2: Waveforms of ideal switching network. (a) gate-to-source voltage of switch (b) switch current, and (c) diode voltage.

The inductor current is

$$I_L = \frac{I_O}{1-D} = \frac{V_O}{R_L(1-D)}. \tag{2.7}$$

Fig. 2.3 shows the linearized dc and low frequency model of buck dc-dc converter. Inductor is a short circuited and filter capacitor is open circuited in the dc model. This model describes the behavior of the converter at steady-state. The efficiency of the converter is

$$\begin{aligned} \eta &= \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = M_{IDC} M_{VDC} \\ &= \frac{1}{1 + \dfrac{r_L + D r_{DS}}{(1-D)^2 R_L} + \dfrac{R_F + D r_C}{(1-D) R_L} + \dfrac{V_F}{V_O} + \dfrac{f_s C_o R_L (1 + M_{VDC})^2}{M_{VDC}^2}}, \end{aligned} \tag{2.8}$$

where r_L, r_{DS}, V_F, R_F, r_C, C_o are the parasitic resistance of the inductor, ON-state resistance of the MOSFET, forward voltage of the diode, forward resistance of the diode, equivalent series resistance of the filter capacitor, and output capacitance of

the MOSFET, respectively.

2.2 Small-Signal Model of PWM Buck-Boost Converter in CCM

The dc model is perturbed about the dc operating point resulting in large-signal nonlinear model. The large-signal quantities can be expressed as the sum of dc and ac components as

$$i_S = I_S + i_s, \tag{2.9}$$

$$i_L = I_L + i_l, \tag{2.10}$$

$$v_D = V_D + v_d, \tag{2.11}$$

$$v_I = V_I + v_i, \tag{2.12}$$

$$v_O = V_O + v_o, \tag{2.13}$$

and

$$d_T = D + d, \tag{2.14}$$

where i_S, i_L, v_D, v_I, v_O, and d_T are the large-signal switch current, inductor current, diode voltage, input voltage, output voltage and duty cycle, respectively. The quantities i_s, i_l, v_d, v_i, v_o, and d are the small-signal switch current, inductor current, diode voltage, input voltage, output voltage and duty cycle, respectively. Hence from (2.1)

$$i_S = d_T i_L = (D + d)(I_L + i_l) \tag{2.15}$$

and from (2.2)

$$v_D = d_T(v_I - v_O) = (D + d)[(V_I + v_i) - (V_O - v_o)]. \tag{2.16}$$

In (2.15) and (2.16), the high-order ac terms are eliminated by using the small-signality conditions yielding a linearized large-signal model. The dc and ac terms are separated to obtain the dc, averaged model as shown in Fig. 2.3 and the linear,

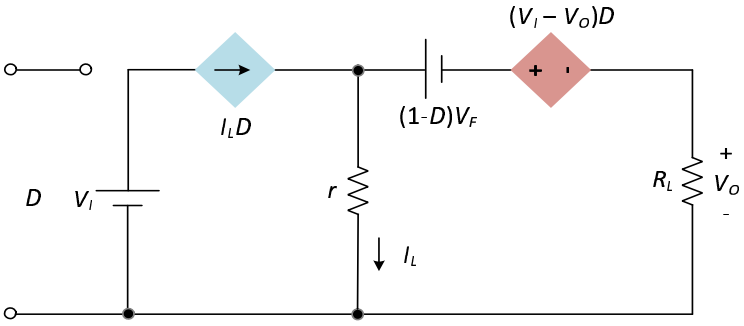

Figure 2.3: DC and low-frequency model of the pulse-width modulated buck-boost dc-dc converter.

Table 2.1: Summary of calculated values for open-loop dc quantities.

Variable	**Value**
I_I	0.8333 A
I_O	2 A
M_{IDC}	2.4
M_{VDC}	0.4167
I_L	2.9470 A
I_S	0.9470 A
V_D	5.4627 V

averaged small-signal model as shown in Fig. 2.4. The equivalent averaged resistance r connected in series with the magnetizing inductance L is given as

$$r = Dr_{DS} + (1 - D)R_F + r_L. \tag{2.17}$$

2.3 Design Example

The subsequent analysis is done on the buck-boost converter designed for the following specifications:

1. Supply voltage $V_I = 12$ V.

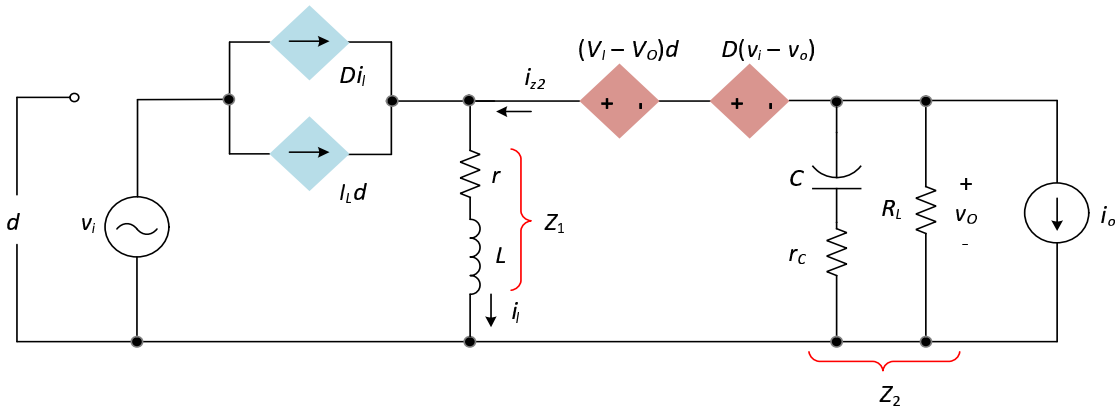

Figure 2.4: Small-signal model of the pulse-width modulated buck-boost dc-dc converter in continuous-conduction mode (CCM).

2. Output voltage $V_O = 5$ V.

3. Output power $P_O = 10$ W.

4. Load resistance $R_L = 2.5\ \Omega$.

5. Switching frequency $f_s = 200$ kHz.

6. Inductance to ensure CCM operation $L = 10\ \mu$H.

7. Filter capacitance $C = 120\ \mu$F.

The equivalent series resistances of the inductor is $r_L = 1\ \text{m}\Omega$ and the capacitor is $r_C = 1\ \text{m}\Omega$. The selected MOSFET was IRF540 by International Rectifiers and the selected diode was MBR10100 by Vishay Semiconductors. From their respective datasheets, the ON-state resistance of the MOSFET and the ON-resistance of the diode were $r_{DS} = 0.11\ \Omega$ and $R_F = 0.07\ \Omega$. Diode forward voltage is $V_F = 0.3$ V. The calculated value of converter efficiency is $\eta = 88\%$. The required duty cycle to achieve the rated output voltage is $D = 0.3213$. The equivalent averaged resistance $r \approx 0.1\ \Omega$. The open-loop dc quantities from Section 2.1 are given in Table 2.1.

2.4 Open-Loop, Closed-Inner Loop, and Closed-Outer Loop Transfer Functions

The transfer functions derived henceforth can be defined and categorized in two ways:

1. Control transfer functions
2. Disturbance transfer functions

The control transfer functions are created by the critical path of open-loop and closed-loop systems. The control variables are duty cycle in open-loop, inner-loop current reference for closed-inner loop, and voltage reference for closed-outer loop transfer functions. The control transfer functions relate the control variables with the output variables such as inductor current and output voltage. These transfer functions are required to determine the following characteristics of a power supply:

- Open-loop and closed-loop bandwidth (also termed as control bandwidth or speed).
- Stability in terms of phase margin and gain margin.
- Magnitude of correction the critical path can provide for disturbances in the input voltage and load current.

On the other hand, the disturbance transfer functions relate the output variable such as inductor current for closed-inner loop or output voltage for closed-voltage loop with the disturbance variable such as input voltage or load current. The parameters of these transfer functions must exhibit the following features:

- Audio susceptibility or the power supply disturbance rejection capability.
- Stability information and attenuation capabilities of the converter output voltage for change in the load current.

- Identify the behavior of the input current caused by changes in the input voltage.

In the following sections, the analytical derivations of important control and disturbance transfer functions for the buck-boost dc-dc converters are presented for the power stage, closed-inner loop, and closed-outer voltage loop. The magnitude and phase plots of these transfer functions and step responses are discussed using MATLAB. Then, the theoretically predicted results are validated using circuit simulations performed on SABER.

2.5 Power Stage Transfer Functions

The following power stage transfer functions are discussed in the subsequent section:

1. Duty cycle-to-output voltage transfer function T_p (Control).
2. Duty cycle-to-inductor current transfer function T_{pi} (Control).
3. Input voltage-to-output voltage transfer function M_v (Disturbance).
4. Input voltage-to-inductor current transfer function M_{vi} (Disturbance).
5. Reverse current gain A_i (Disturbance).
6. Input impedance Z_i (Disturbance).
7. Output impedance Z_o (Disturbance).

The small-signal model of the PWM buck-boost converter is shown in Fig. 2.4. The current through the parallel combination of the load resistance and the filter capacitor is

$$i_{Z2} = \frac{v_o}{Z_2}. \tag{2.18}$$

The input and the switch currents are

$$i_i = i_s = Di_l + I_L d. \tag{2.19}$$

The current through the inductor is

$$i_l = i_s + i_{Z2} = Di_l + I_L d + i_{Z2} = Di_l + I_L d + \frac{v_o}{Z_2} = \frac{I_L d}{1-D} + \frac{v_o}{Z_2(1-D)}. \quad (2.20)$$

Applying Kirchhoff's voltage law, the output voltage is

$$v_o = (V_I + V_O)d + D(v_i + v_o) - i_l Z_1. \quad (2.21)$$

The impedances Z_1 and Z_2 are

$$Z_1 = r + sL \quad (2.22)$$

and

$$Z_2 = R_L || \left(r_c + \frac{1}{sC} \right) = \frac{R_L \left(r_C + \frac{1}{sC} \right)}{R_L + r_C + \frac{1}{sC}}. \quad (2.23)$$

2.5.1 Duty Cycle-to-Output Voltage Transfer Function T_p

The duty cycle-to-output voltage transfer function is obtained by setting $v_i = 0$ and $i_o = 0$ in Fig. 2.4. Setting $v_i = 0$ in (2.21) and rearranging

$$v_o = (V_I + V_O)d + Dv_o - i_l Z_1. \quad (2.24)$$

Substituting (2.20) in (2.24)

$$v_o = (V_I + V_O)d + Dv_o - \left[\frac{I_L d}{1-D} + \frac{v_o}{Z_2(1-D)} \right] Z_1, \quad (2.25)$$

yielding

$$v_o(1-D) = (V_I + V_O)d - \frac{I_L d}{1-D} Z_1 - \frac{v_o}{Z_2(1-D)} Z_1 \quad (2.26)$$

and

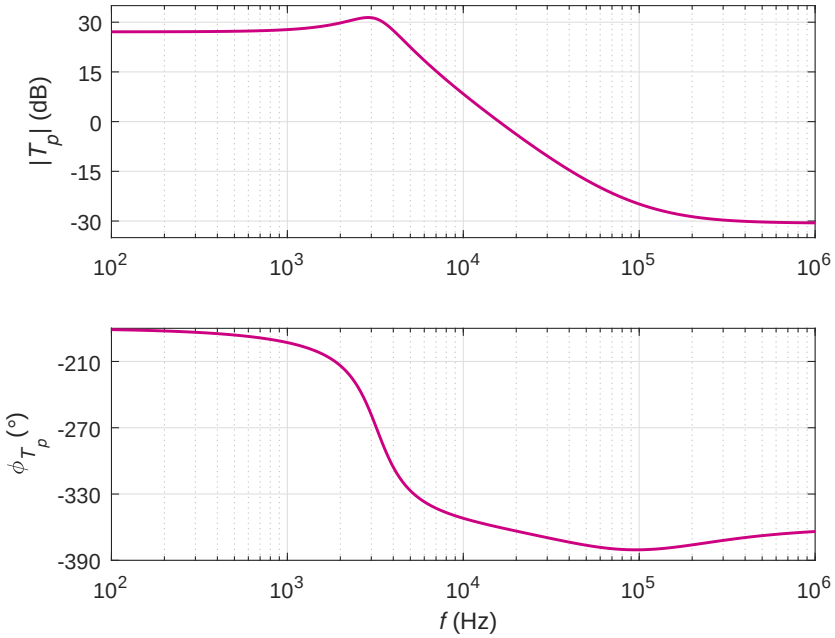

Figure 2.5: Theoretically obtained magnitude and phase plots of the duty cycle-to-output voltage transfer function T_p.

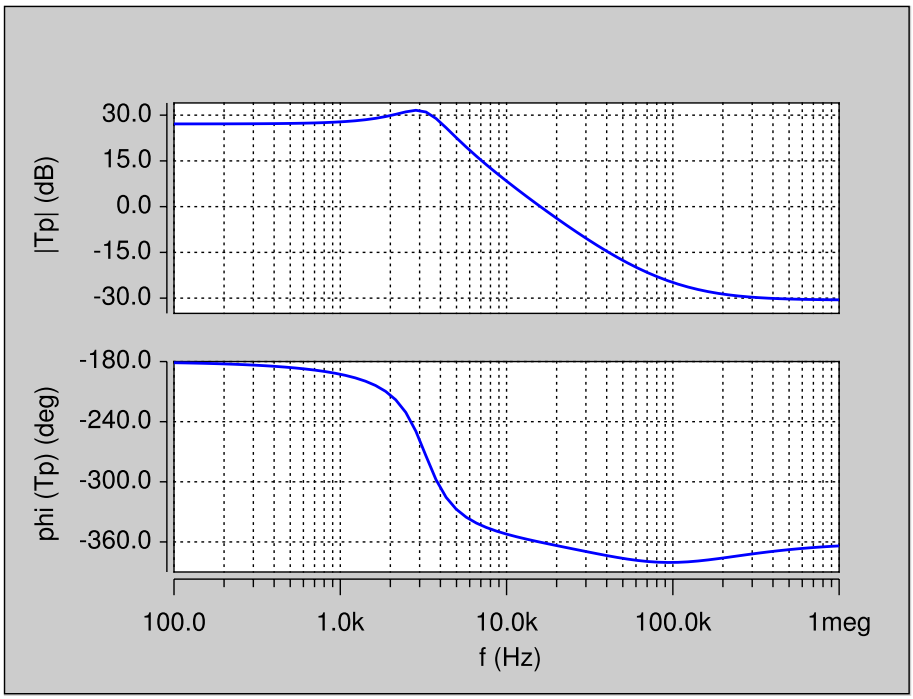

Figure 2.6: Magnitude and phase plots of the duty cycle-to-output voltage transfer function T_p obtained by circuit simulations.

$$v_o\left[(1-D)+\frac{Z_1}{Z_2(1-D)}\right]=d\left[(V_I+V_O)-\frac{I_L}{1-D}Z_1\right]. \tag{2.27}$$

Hence, the control-to-output transfer function is

$$\begin{aligned} T_p(s)=&\left.\frac{v_o(s)}{d(s)}\right|_{v_i=i_o=0}\\ =&\frac{(V_I+V_O)(1-D)-I_LZ_1}{1-D}\ \ \frac{Z_2(1-D)}{Z_1+Z_2(1-D)^2}\\ =&\frac{[(V_I+V_O)(1-D)-I_LZ_1]Z_2}{Z_1+Z_2(1-D)^2}. \end{aligned} \tag{2.28}$$

Substituting (2.22) and (2.23) in (2.28) gives the control-to-output transfer function in s-domain as

$$T_p(s)=\left.\frac{v_o(s)}{d(s)}\right|_{v_i=i_o=0}=T_{px}\frac{(s+\omega_{zn})(s-\omega_{zp})}{s^2+2\xi\omega_0 s+\omega_0^2}=T_{po}\frac{\left(1+\dfrac{s}{\omega_{zn}}\right)\left(1-\dfrac{s}{\omega_{zp}}\right)}{\left(\dfrac{s}{\omega_0}\right)^2+\dfrac{2\xi s}{\omega_0}+1}, \tag{2.29}$$

where the dc gain T_{po} is

$$T_{po}=\frac{V_o r-(1-D)^2(V_I+V_O)R_L}{(1-D)[r+R_L(1-D)^2]}, \tag{2.30}$$

the gain T_{px} is

$$T_{px}=-\frac{V_O}{1-D}\ \frac{r_C}{R_L+r_C}, \tag{2.31}$$

the angular corner frequency or the angular undamped natural frequency is

$$\omega_0=\sqrt{\frac{r+R_L(1-D)^2}{LC(R_L+r_C)}}, \tag{2.32}$$

and the damping ratio is

$$\xi=\frac{rC(R_L+r_C)+L+R_Lr_CC(1-D)^2}{2\sqrt{LC(R_L+r_C)[r+R_L(1-D)^2]}}. \tag{2.33}$$

The angular frequency of the left-half plane zero is

$$\omega_{zn}=\frac{1}{r_CC} \tag{2.34}$$

and the angular frequency of the right-half plane zero is

$$\omega_{zp} = \frac{(1-D)^2(V_I + V_O)R_L - V_O r}{LV_O} = \frac{(1-D)^2 R_L - Dr}{DL}. \tag{2.35}$$

Fig. 2.5 shows the theoretically obtained magnitude and phase plots of duty cycle-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 2.6 shows the magnitude and phase plots of duty cycle-to-output voltage transfer function using SABER Simulator. The gain at dc and low-frequencies is nearly $T_{p0} = 27.1$ dB $= 22.63$ V/V. The natural corner frequency of the second-order low-pass filter formed by the inductor, capacitor, and load resistor is $f_o = 3.24$ kHz. The gain decreases by 40 dB/dec beyond f_o. The duty cycle-to-output voltage transfer function of the buck-boost converter exhibits a right-half plane (RHP) zero located at $f_{zp} = \omega_{zp}/2\pi$. The RHP zero is a zero for magnitude but behaves like a pole for phase. The RHP zero cancels the effect of one of the complex conjugate poles reducing the fall-off slope to -20 dB/dec. Beyond f_{zp}, the gain decreases by -20 dB/dec and is finally canceled by the left-half plane zero (LHP) zero $f_{zn} = \omega_{zn}/2\pi$ created by the capacitor C and its resistance r_C. The gain at high frequencies is constant and equal to -30 dB at high frequencies. The zero frequency is caused by the series combination of the filter capacitance and the equivalent series resistance of the filter capacitance. The phase is $-180°$ at dc and low frequencies indicating a phase inversion between the duty cycle and the output voltage, i.e., as duty cycle increases or decreases, the output voltage decreases or increases, respectively. With increase in frequency, the phase rolls off by $-180°$ per decade due to the complex conjugate poles. In addition, the presence of the RHP zero adds an additional phase of $-45°$ per decade at f_{zp}, thereby having the phase cross $-360°$. At high frequencies, the effect on pole (or RHP zero) is nullified by the LHP zero and phase begins to roll-up towards $-270°$.

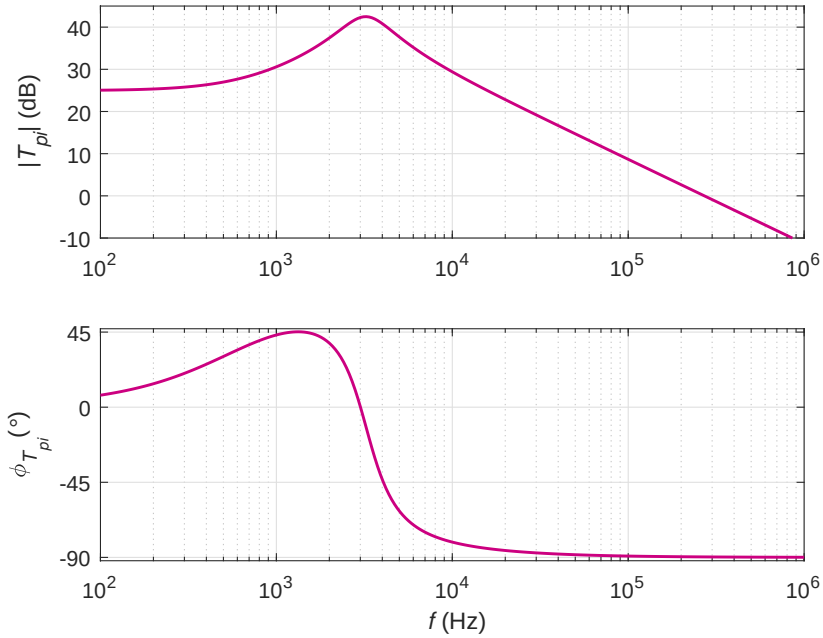

Figure 2.7: Theoretically obtained magnitude and phase plots of the duty cycle-to-inductor current transfer function T_{pi}.

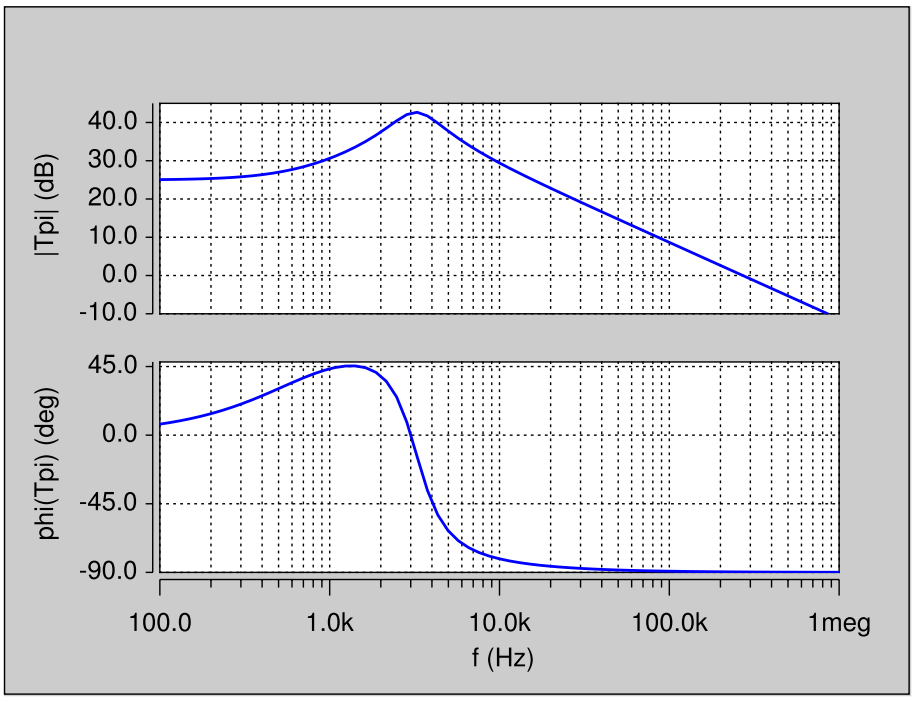

Figure 2.8: Magnitude and phase plots of the duty cycle-to-inductor current transfer function T_{pi} obtained by circuit simulation.

2.5.2 Duty Cycle-to-Inductor Current Transfer Function T_{pi}

The duty cycle-to-output voltage transfer function is obtained by setting $v_i = 0$ and $i_o = 0$ in Fig. 2.4. Setting $v_i = 0$ in (2.21) and rearranging

$$v_o = (V_I + V_O)d + Dv_o - i_l Z_1 = \frac{(V_I + V_O)d}{1 - D} - \frac{i_l Z_1}{1 - D}. \tag{2.36}$$

Substituting (2.36) into (2.20) yields

$$i_l = \frac{I_L d}{1 - D} + \frac{(V_I + V_O)d}{Z_2(1 - D)^2} - \frac{i_l Z_1}{Z_2(1 - D)^2}. \tag{2.37}$$

Rearranging (2.37)

$$i_l + \frac{i_l Z_1}{Z_2(1 - D)^2} = \frac{I_L d}{1 - D} + \frac{(V_I + V_O)d}{Z_2(1 - D)^2}, \tag{2.38}$$

which becomes

$$i_l \left[1 + \frac{Z_1}{Z_2(1 - D)^2}\right] = d\left[\frac{I_L}{1 - D} + \frac{(V_I + V_O)}{Z_2(1 - D)^2}\right]. \tag{2.39}$$

Hence, the control-to-inductor current transfer function is

$$T_{pi}(s) = \left.\frac{i_l(s)}{d(s)}\right|_{v_i = i_o = 0} = \frac{\dfrac{I_L}{1 - D} + \dfrac{(V_I + V_O)}{Z_2(1 - D)^2}}{1 + \dfrac{Z_1}{Z_2(1 - D)^2}} = \frac{(V_I + V_O) + I_L(1 - D)Z_2}{Z_1 + (1 - D)^2 Z_2}. \tag{2.40}$$

Substituting (2.22) and (2.23) in (2.40) gives the control-to-inductor current transfer function in s-domain as

$$T_{pi}(s) = \left.\frac{i_l(s)}{d(s)}\right|_{v_i = i_o = 0} = T_{pix}\frac{s + \omega_{zi}}{s^2 + 2\xi\omega_0 s + \omega_0^2} = T_{pio}\frac{1 + \dfrac{s}{\omega_{zi}}}{\left(\dfrac{s}{\omega_0}\right)^2 + \dfrac{2\xi s}{\omega_0} + 1}, \tag{2.41}$$

where the dc gain T_{pio} is

$$T_{pio} = \frac{2V_O + V_I}{r + R_L(1 - D)^2}, \tag{2.42}$$

the gain T_{pix} is

$$T_{pix} = \frac{V_O r_C + (V_I + V_O)(R_L + r_C)}{L(R_L + r_C)}, \tag{2.43}$$

and the angular frequency of the left-half plane zero is

$$\omega_{zi} = \frac{1+D}{C[r_C(1+D)+R_L]}. \tag{2.44}$$

Fig. 2.7 shows the theoretically obtained magnitude and phase plots of the control-to-inductor current transfer function. The theoretical results were validated by simulation. Fig. 2.8 shows the magnitude and phase plots of the control-to-inductor current transfer function using SABER Simulator. The gain at dc and low-frequencies is nearly $T_{pi0} = 17.8$ dB $= 25$ A/V. The natural corner frequency of the second-order low-pass filter formed by the inductor, capacitor, and load resistor is $f_o = 3.24$ kHz. The transfer function exhibits a LHP zero $f_{zi} = \omega_{zi}/2\pi$ and a pair of complex conjugate poles at f_o. The frequency of the LHP zero f_{zi} is inversely proportional to the filter capacitance and the load resistance. Beyond f_o The gain decreases at the rate of 20 dB/dec. The phase starts at zero and rises to 45° due to f_{zi}. This means that at low frequencies, the duty cycle signal leads the inductor current by a particular phase angle. The bandwidth of T_{pi} is larger than that of T_p. Therefore, the inner-current loop presents a faster response in inductor current for change in duty cycle. The low-frequency zero f_{zi} depends on the load resistance R_L and the parameters of the filter capacitance, namely C and r_C. As the value of R_L is decreased at a fixed C, f_{zi} moves towards f_o. The nature of the roots of the characteristic equation (denominator of T_{pi}) or the poles of T_{pi} converts from complex conjugate to real. At a specific minimum load resistance, $f_{zi} \approx f_o$, i.e., f_{zi} cancels the effect of one of the complex conjugate poles at f_o producing a first-order dominant pole system. The dominant pole is therefore caused by the inductor and load resistance.

2.5.3 Input Voltage-to-Output Voltage Transfer Function M_v

The input voltage-to-output voltage transfer function is obtained by setting $d = 0$ and $i_o = 0$ in Fig. 2.4. Setting $d = 0$ in (2.21) and rearranging

$$v_o = Dv_i + Dv_o - i_l Z_1, \tag{2.45}$$

which becomes

$$v_o(1 - D) = Dv_i - i_l Z_1. \tag{2.46}$$

Setting $d = 0$ in (2.20) and rearranging, we get

$$i_l = i_s + i_{Z2} = Di_l + i_{Z2} = Di_l + \frac{v_o}{Z_2}. \tag{2.47}$$

Rearranging (2.47)

$$i_l(1 - D) = \frac{v_o}{Z_2}, \tag{2.48}$$

$$i_l = \frac{v_o}{(1 - D)Z_2}. \tag{2.49}$$

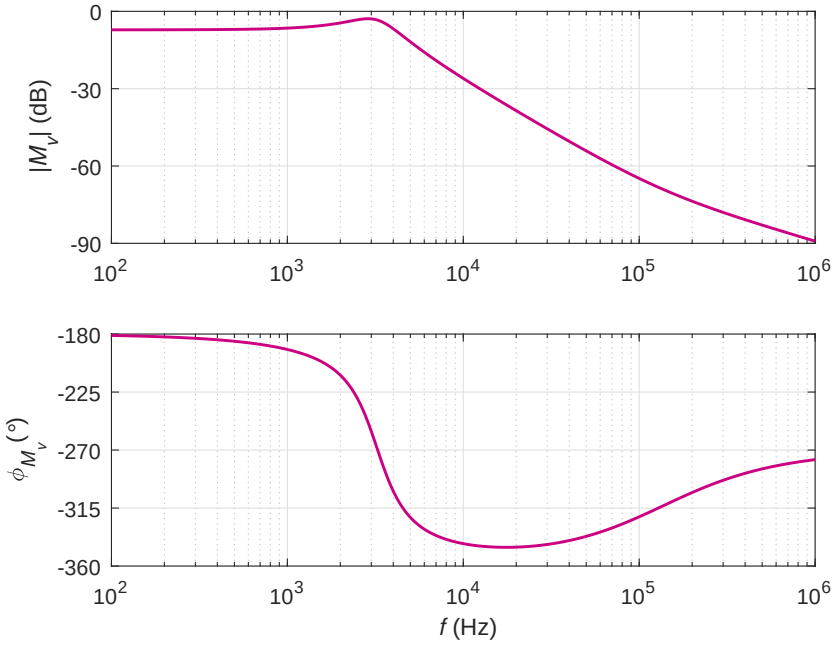

Figure 2.9: Theoretically obtained magnitude and phase plots of the input voltage-to-output voltage transfer function M_v.

Substituting (2.49) in (2.46)

$$v_o(1-D) = Dv_i - Z_1\frac{v_o}{(1-D)Z_2}. \tag{2.50}$$

Rearranging further,

$$v_o\left[(1-D) + \frac{Z_1}{(1-D)Z_2}\right] = Dv_i. \tag{2.51}$$

Hence, the input voltage-to-output voltage transfer function M_v

$$M_v(s) = \left.\frac{v_o(s)}{v_i(s)}\right|_{d=i_o=0} = \frac{D}{\frac{Z_2(1-D)^2 + Z_1}{(1-D)Z_2}} = \frac{D(1-D)Z_2}{Z_1 + Z_2(1-D)^2}. \tag{2.52}$$

Substituting (2.22) and (2.23) in (2.40) gives the input voltage-to-output voltage transfer function in s-domain as

$$M_v(s) = \left.\frac{v_o(s)}{v_i(s)}\right|_{d=i_o=0} = M_{vx}\frac{s+\omega_{zn}}{s^2 + 2\xi\omega_0 s + \omega_0^2} = -M_{vo}\frac{1 + \frac{s}{\omega_{zn}}}{\left(\frac{s}{\omega_0}\right)^2 + \frac{2\xi s}{\omega_0} + 1}, \tag{2.53}$$

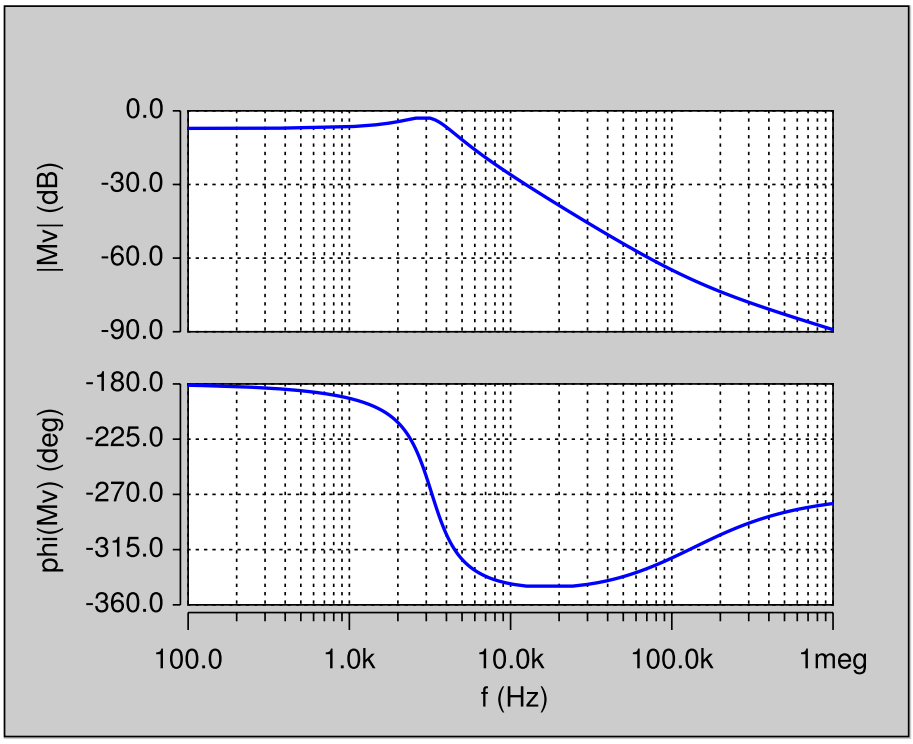

Figure 2.10: Magnitude and phase plots of the input voltage-to-output voltage transfer function M_v obtained by circuit simulation.

where the dc gain M_{vo} is

$$M_{vo} = \frac{R_L(1-D)D}{R_L(1-D)^2 + r} \approx \frac{D}{1-D} \tag{2.54}$$

and the gain M_{vx} is

$$M_{vx} = \frac{R_L r_C(1-D)D}{L(R_L + r_C)}. \tag{2.55}$$

The angular frequency of the left-half plane zero ω_{zn} is given in (2.34).

Fig. 2.9 shows the theoretically obtained magnitude and phase plots of the input voltage-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 2.10 shows the magnitude and phase plots of the input voltage-to-output voltage transfer function using SABER Simulator. The gain at dc is nearly equal to the duty cycle $M_{vo} = -7.2$ dB $= 0.438$ V/V. The gain at dc is mainly dependent on duty cycle. The gain at dc is below 0 dB for the buck mode and is above 0 dB for the boost mode. In the buck-boost converter, any change in the input voltage causes a change in the output voltage during the switch ON interval. In addition, the changes in the input and output voltages take place in opposite directions resulting in $-180°$ phase shift at dc and low frequencies. The phase starts at zero and decreases towards $-180°$. However, the high-frequency LHP zero at ω_z increases the phase to $90°$.

2.5.4 Input Voltage-to-Inductor Current Transfer Function M_{vi}

The input voltage-to-inductor current transfer function is obtained by setting $d = 0$ and $i_o = 0$ in Fig. 2.4. Setting $d = 0$ in (2.21) and rearranging

$$v_o = Dv_i + Dv_o - Z_1 i_l, \tag{2.56}$$

which becomes

$$v_o = \frac{Dv_i - Z_1 i_l}{1-D}. \tag{2.57}$$

Setting $d = 0$ in (2.20) and rearranging, we get

$$i_l = i_s + i_{Z2} = Di_l + i_{Z2} = Di_l + \frac{v_o}{Z_2} \tag{2.58}$$

and

$$i_l(1 - D) = \frac{v_o}{Z_2}. \tag{2.59}$$

Substituting (2.57) in (2.59)

$$i_l(1 - D) = \frac{Dv_i - Z_1 i_l}{Z_2(1 - D)}. \tag{2.60}$$

Rearranging,

$$i_l\left[(1 - D) + \frac{Z_1}{Z_2(1 - D)}\right] = \frac{Dv_i}{Z_2(1 - D)}. \tag{2.61}$$

Hence, the input voltage-to-inductor current transfer function M_{vi} is

$$M_{vi}(s) = \left.\frac{i_l(s)}{v_i(s)}\right|_{d=i_o=0} = \frac{D}{Z_1 + Z_2(1 - D)^2}. \tag{2.62}$$

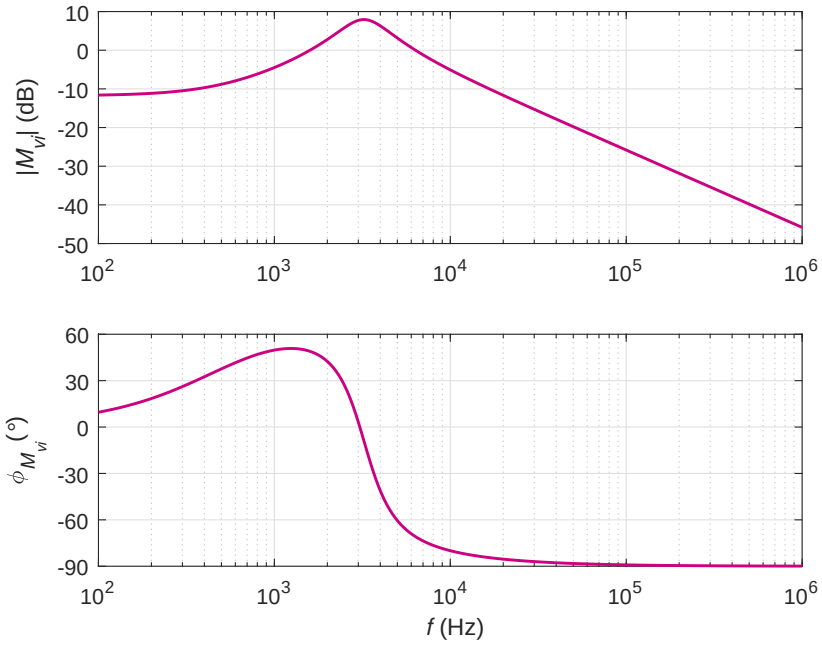

Figure 2.11: Theoretically obtained magnitude and phase plots of input voltage-to-inductor current transfer function M_{vi}.

Substituting (2.22) and (2.23) in (2.62) gives the input voltage-to-inductor current transfer function in s-domain as

$$M_{vi}(s) = \frac{i_l(s)}{v_i(s)}\bigg|_{d=i_o=0} = M_{vix}\frac{s+\omega_{zvi}}{s^2+2\xi\omega_0 s+\omega_0^2} = M_{vio}\frac{1+\dfrac{s}{\omega_{zvi}}}{\left(\dfrac{s}{\omega_0}\right)^2+\dfrac{2\xi s}{\omega_0}+1}, \tag{2.63}$$

where the dc gain M_{vio} is

$$M_{vio} = \frac{D}{r+R_L(1-D)^2}, \tag{2.64}$$

the gain M_{vix} is

$$M_{vix} = \frac{D}{L}, \tag{2.65}$$

and the angular frequency of the left-half plane zero is

$$\omega_{zvi} = \frac{1}{C(R_L+r_C)}. \tag{2.66}$$

Fig. 2.11 shows the theoretically obtained magnitude and phase plots of the input voltage-to-inductor current transfer function. The theoretical results were validated

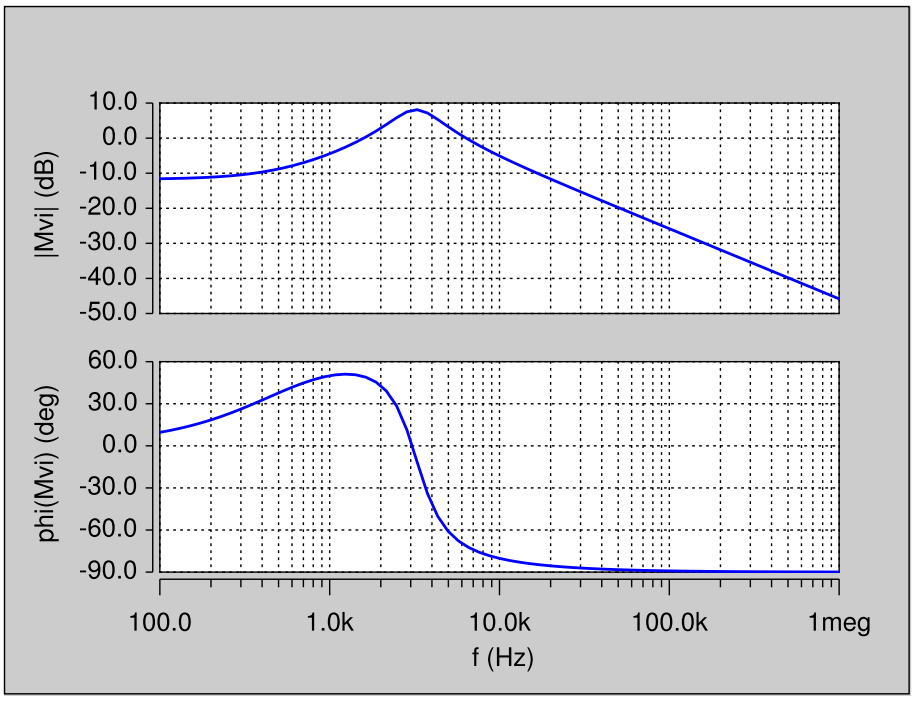

Figure 2.12: Magnitude and phase plots of input voltage-to-inductor current transfer function M_{vi} obtained by circuit simulation.

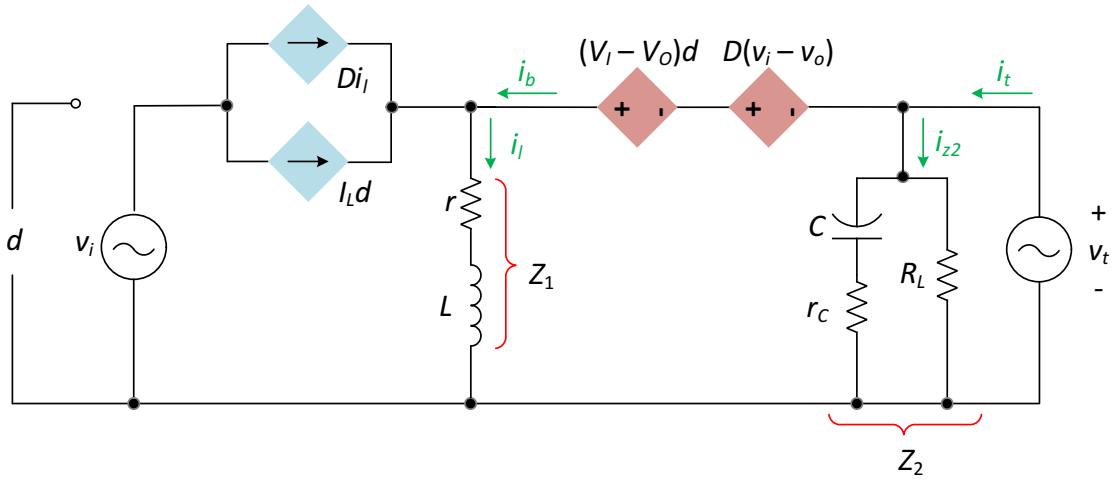

Figure 2.13: Small-signal model of the pulse-width modulated buck-boost dc-dc converter in CCM to derive output current-to-inductor current transfer function A_i.

by simulation. Fig. 2.12 shows the magnitude and phase plots of the input voltage-to-inductor current transfer function using SABER Simulator. The gain at dc is $M_{vi0} = -11.8\text{dB} = 0.2582\text{A/V}$. Through the M_{vi} current-loop relevant transfer function, one can observe that the current loop offers a low audio susceptibility at dc than that provided by the voltage-loop transfer function M_v. All the other frequency-domain properties remain identical to T_{pi}.

2.5.5 Reverse Current Gain A_i

The small-signal model to derive output-to-inductor current transfer function is shown in Fig. 2.13. This model is obtain by setting $v_i = 0$ and $d = 0$. An independent voltage source v_t is applied at the output, which forces a current i_t. Applying Kirchhoff's voltage law,

$$v_t = (V_I + V_O)d + D(v_i + v_t) - i_l Z_1. \tag{2.67}$$

Setting $v_i = 0$ and $d = 0$ in (2.67),

$$v_t = Dv_t - i_l Z_1 = -\frac{i_l Z_1}{(1-D)}. \tag{2.68}$$

Applying Kirchoff's current law

$$i_l = I_L d + D i_l + i_b. \tag{2.69}$$

By setting $d = 0$ in (2.69), we get

$$i_l = D i_l + i_b. \tag{2.70}$$

Hence

$$i_b = i_l(1 - D). \tag{2.71}$$

The current i_t is given as

$$i_t = -i_o = i_{Z2} + i_b = -\frac{v_t}{Z_2} + i_l(1 - D). \tag{2.72}$$

Substituting (2.68) in above equation

$$-i_o = \frac{i_l Z_1}{Z_2(1 - D)} + i_l(1 - D) = i_l\left[\frac{Z_1}{Z_2(1 - D)} + (1 - D)\right]. \tag{2.73}$$

Hence, the output current-to-inductor current transfer function or reverse current transfer function A_i is

$$A_i(s) = \left.\frac{i_l(s)}{i_o(s)}\right|_{d=v_i=0} = -\frac{1}{\dfrac{Z_1}{(1 - D)Z_2} + (1 - D)}. \tag{2.74}$$

Substituting (2.22) and (2.23) in (2.74) gives the output current-to-inductor current transfer function in s-domain as

$$A_i(s) = \left.\frac{i_l(s)}{i_o(s)}\right|_{d=v_i=0} = A_{ix}\frac{s + \omega_{zn}}{s^2 + 2\xi\omega_0 s + \omega_0^2} = A_{io}\frac{1 + \dfrac{s}{\omega_{zn}}}{\left(\dfrac{s}{\omega_0}\right)^2 + \dfrac{2\xi s}{\omega_0} + 1}, \tag{2.75}$$

where the dc gain A_{io} is

$$A_{io} = \frac{(1 - D)R_L}{[r + R_L(1 - D)^2]}, \tag{2.76}$$

the gain A_{ix} is

$$A_{ix} = \frac{(1 - D)R_L r_C}{L(R_L + r_C)}, \tag{2.77}$$

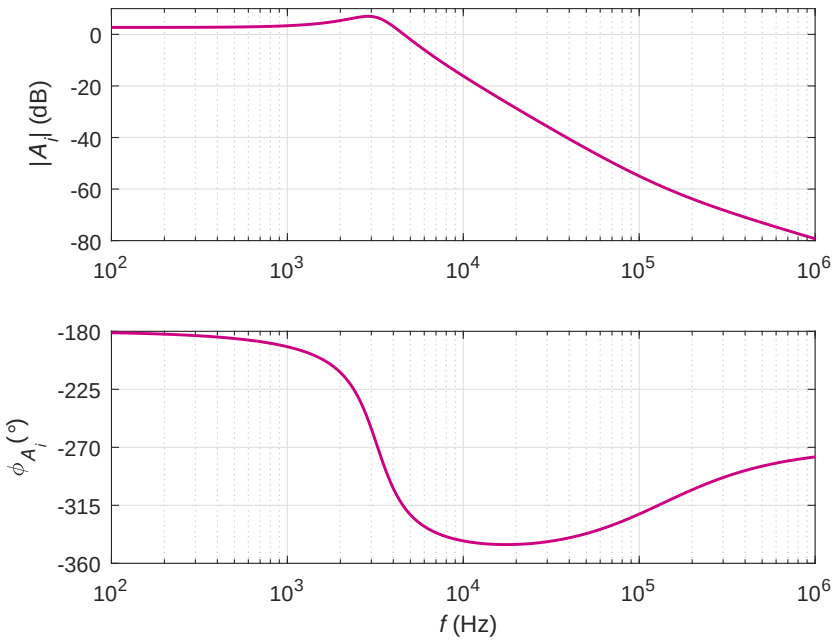

Figure 2.14: Theoretically obtained magnitude and phase plots of the output current-to-inductor current transfer function A_i.

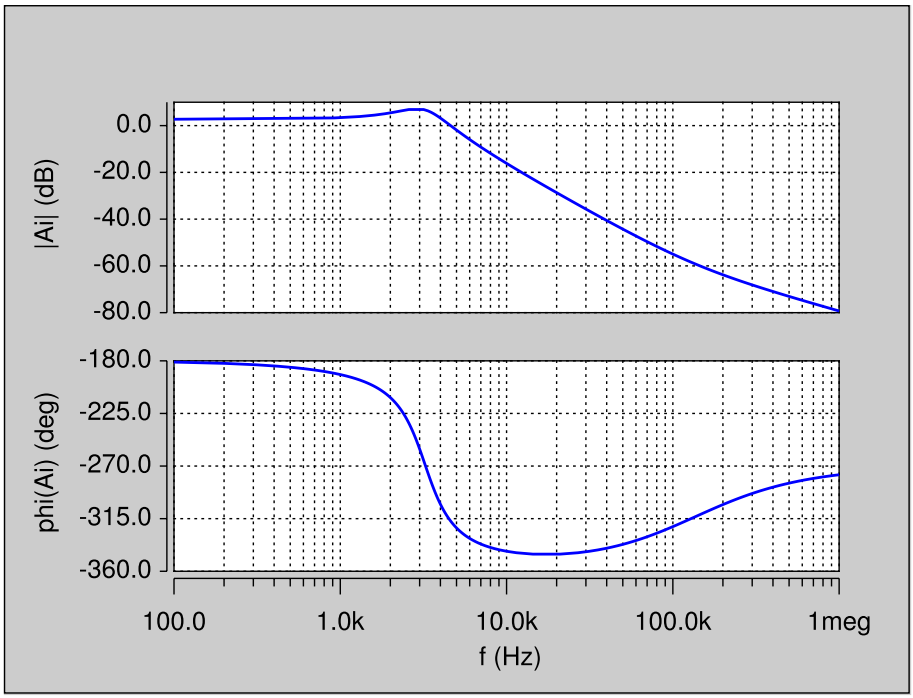

Figure 2.15: Magnitude and phase plots of the output current-to-inductor current transfer function A_i obtained by circuit simulation.

and the angular frequency of the left-half plane zero ω_{zn} is given in (2.34).

Fig. 2.14 shows the theoretically obtained magnitude and phase plots of the output current-to-inductor current transfer function. The theoretical results were validated by simulation. Fig. 2.15 shows the magnitude and phase plots of the output current-to-inductor current transfer function using SABER Simulator. The gain at dc is $A_{i0} = 0$ dB = 1 A/A, i.e., the reverse current gain is unity at dc and low-frequencies up to nearly f_o. Beyond f_o the impedance offered by the capacitor branch is lower than the inductor and the small-signal output current begins to flow into the capacitor. Therefore, the gain reduces by 20 dB per decade.

2.5.6 Open-Loop Input Impedance Z_i

The open-loop input impedance is obtained by setting $d = 0$ and $i_o = 0$ in (2.21) and (2.20) and rearranging as

$$v_o = D(v_i + v_o) - i_l Z_1 = \frac{Dv_i}{1-D} - \frac{i_l Z_1}{1-D} \tag{2.78}$$

and

$$i_l = Di_l + \frac{v_o}{Z_2}, \tag{2.79}$$

yielding

$$i_l(1-D) = \frac{v_o}{Z_2}. \tag{2.80}$$

Rearranging (2.80) becomes

$$v_o = i_l(1-D)Z_2. \tag{2.81}$$

Equating (2.81) and (2.78)

$$i_l(1-D)Z_2 = \frac{Dv_i}{1-D} - \frac{i_l Z_1}{1-D}. \tag{2.82}$$

Rearrangement of the above equation produces

$$i_l\left[(1-D)Z_2 + \frac{Z_1}{1-D}\right] = \frac{Dv_i}{1-D}. \tag{2.83}$$

Setting $d = 0$ in (2.19) input current becomes

$$i_i = Di_l. \tag{2.84}$$

Substituting (2.84) in (2.83), we get

$$\frac{i_i}{D}\left[(1-D)Z_2 + \frac{Z_1}{1-D}\right] = \frac{Dv_i}{1-D}. \tag{2.85}$$

Hence, the open-loop input impedance is

$$Z_i(s) = \left.\frac{v_i(s)}{i_i(s)}\right|_{d=i_o=0} = \frac{Z_1 + (1-D)^2 Z_2}{D^2}. \tag{2.86}$$

Substituting (2.22) and (2.23) in (2.86) gives the output current-to-inductor current transfer function in s-domain as

$$Z_i(s) = \left.\frac{v_i(s)}{i_i(s)}\right|_{d=i_o=0} = Z_{ix}\frac{s^2 + 2\xi\omega_0 s + \omega_0^2}{(s+\omega_{zvi})} = Z_{io}\frac{\left(\frac{s}{\omega_0}\right)^2 + \frac{2\xi s}{\omega_0} + 1}{\left(1 + \frac{s}{\omega_{zvi}}\right)}, \tag{2.87}$$

where the dc gain Z_{io} is

$$Z_{io} = Z_i(0) = R_{io} = \frac{r + R_L(1-D)^2}{D^2}, \tag{2.88}$$

the gain Z_{ix} is

$$Z_{ix} = \frac{L}{D^2}, \tag{2.89}$$

and the angular frequency of the left-half plane zero ω_{zvi} is given in (2.66).

Fig. 2.16 shows the theoretically obtained magnitude and phase plots of the input impedance. The theoretical results were validated by simulation. Fig. 2.17 shows the magnitude and phase plots of the input impedance using SABER Simulator. The input resistance R_{io} at dc is proportional to the duty cycle and the load resistance. With increase in frequency, the input impedance shows capacitive nature. Beyond f_o the inductive reactance takes over and the input impedance is mainly dominated by the inductive reactance. In open-loop condition, the input current is in phase with the input voltage, i.e., a step change in the input voltage in positive direction, causes a corresponding change in the input current in the same direction.

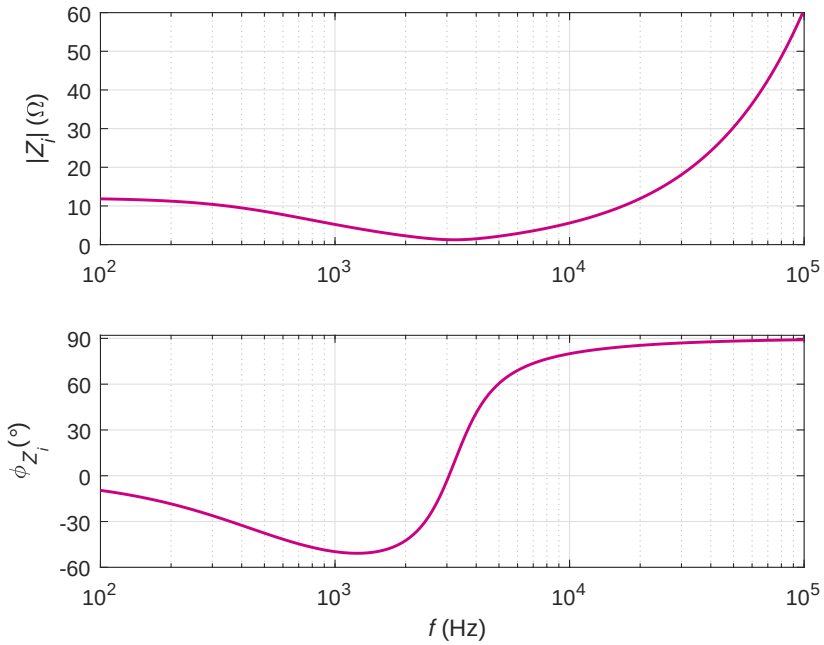

Figure 2.16: Theoretically obtained magnitude and phase plots of the input impedance Z_i.

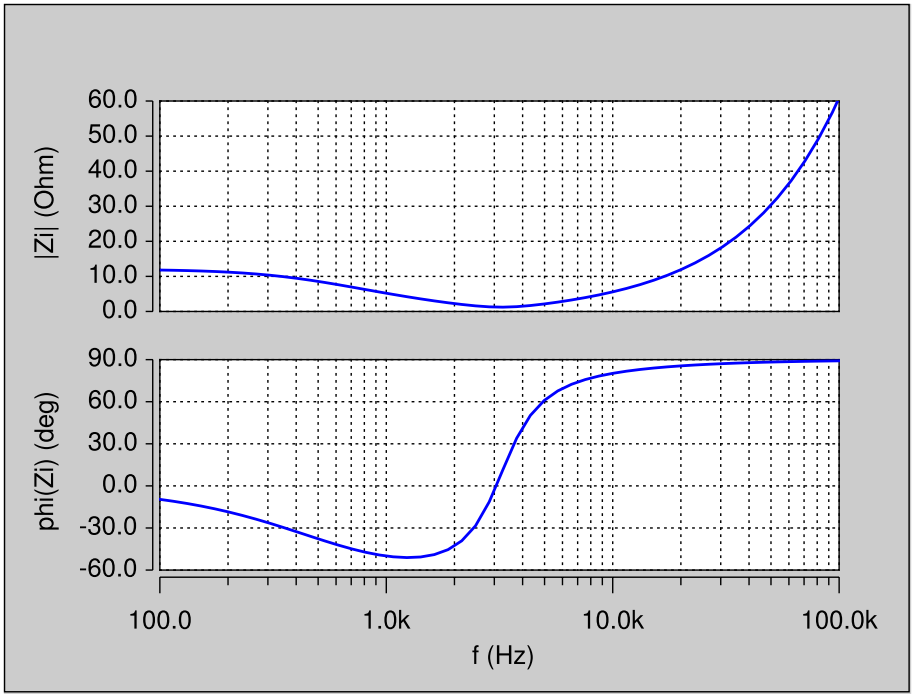

Figure 2.17: Magnitude and phase plots of the input impedance Z_i obtained by circuit simulation.

2.5.7 Open-Loop Output Impedance Z_o

The small-signal model to derive output impedance is shown in Fig. 2.13. This model is obtain by setting $v_i = 0$ and $d = 0$. An independent voltage source v_t is applied at the output, which forces a current i_t. Applying Kirchhoff's voltage law,

$$v_t = (V_I + V_O)d + D(v_i + v_t) - i_l Z_1. \tag{2.90}$$

Setting $v_i = 0$ and $d = 0$ in (2.90),

$$v_t = Dv_t - i_l Z_1. \tag{2.91}$$

Rearranging (2.91)

$$i_l = \frac{-v_t(1-D)}{Z_1}. \tag{2.92}$$

Applying Kirchoff's current law

$$i_l = I_L d + Di_l + i_b. \tag{2.93}$$

By setting $d = 0$ in (2.93)

$$i_l = Di_l + i_b. \tag{2.94}$$

Hence

$$i_l(1-D) = i_b. \tag{2.95}$$

The current i_t is given as

$$i_t = i_{Z2} + i_b = -\frac{v_t}{Z_2} + i_b. \tag{2.96}$$

Rearrangement of (2.96) yields

$$i_b = i_t + \frac{v_t}{Z_2}. \tag{2.97}$$

Substituting (2.97) and (2.92) in (2.95)

$$\frac{-v_t(1-D)}{Z_1}(1-D) = i_t + \frac{v_t}{Z_2}, \tag{2.98}$$

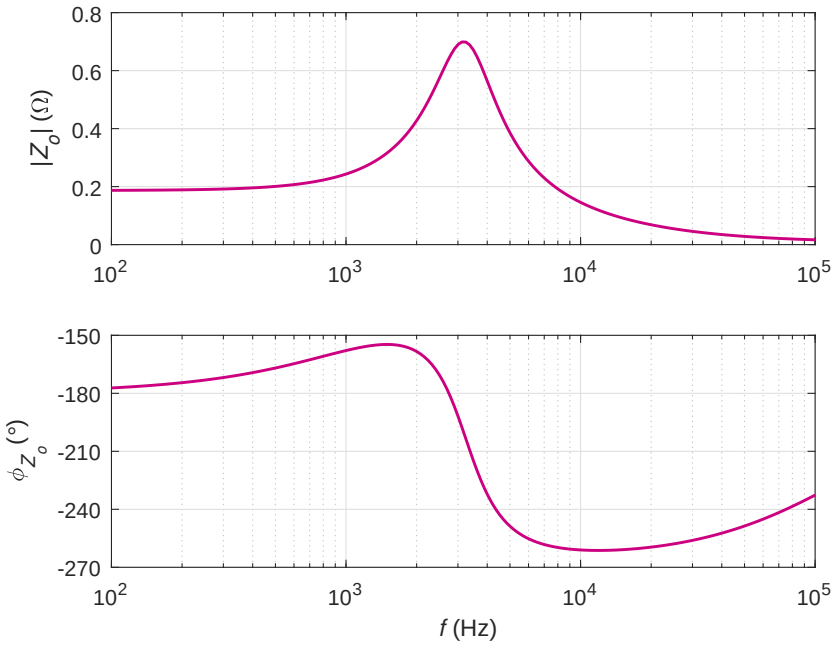

Figure 2.18: Theoretically obtained magnitude and phase plots of the output impedance Z_o.

which becomes

$$v_t\left[\frac{-1}{Z_2}-\frac{(1-D)^2}{Z_1}\right]=i_t. \tag{2.99}$$

Hence

$$\begin{aligned} Z_o(s) &= \left.\frac{v_t(s)}{i_t(s)}\right|_{d=v_i=0} \\ &= -\frac{1}{\dfrac{1}{Z_2}+\dfrac{(1-D)^2}{Z_1}} = -\frac{Z_1Z_2}{Z_1+Z_2(1-D)^2}. \end{aligned} \tag{2.100}$$

The open-loop output impedance is

$$\begin{aligned} Z_o(s) &= -\left.\frac{v_o(s)}{i_o(s)}\right|_{d=v_i=0} \\ &= \frac{Z_1Z_2}{Z_1+Z_2(1-D)^2}. \end{aligned} \tag{2.101}$$

Substituting (2.22) and (2.23) in (2.101) gives the open-loop output impedance in

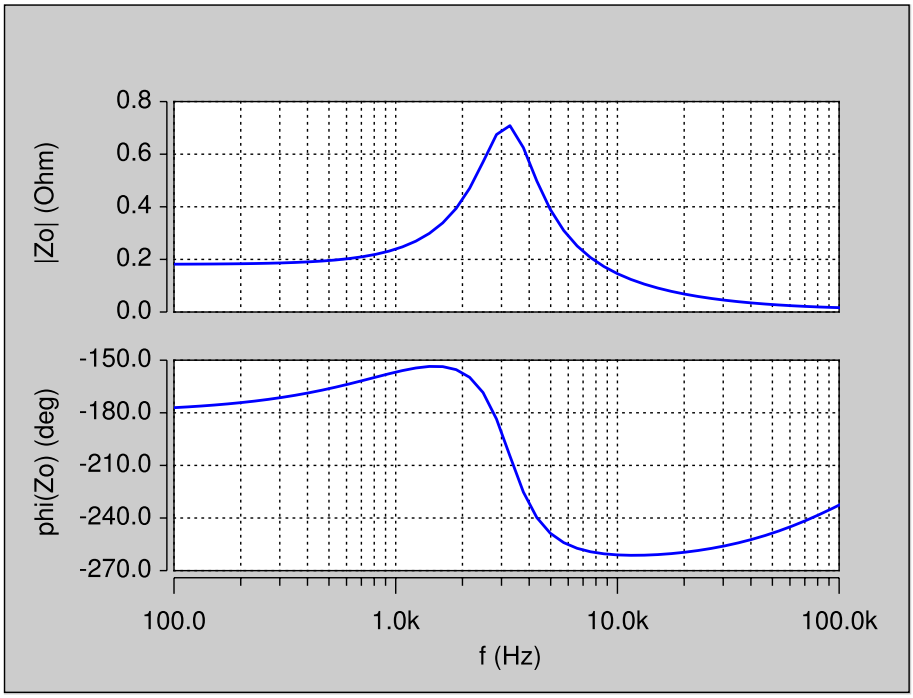

Figure 2.19: Magnitude and phase plots of the output impedance Z_o obtained by circuit simulation.

s-domain as

$$Z_o(s) = \left.\frac{v_o(s)}{i_o(s)}\right|_{d=v_i=0} = Z_{ox}\frac{(s+\omega_{zn})(s+\omega_{rl})}{s^2+2\xi\omega_0 s+\omega_0^2} = Z_{o0}\frac{\left(1+\dfrac{s}{\omega_{zn}}\right)\left(1+\dfrac{s}{\omega_{rl}}\right)}{\left(\dfrac{s}{\omega_0}\right)^2+\dfrac{2\xi s}{\omega_0}+1}, \quad (2.102)$$

where the dc gain Z_{o0} is

$$Z_{o0} = \frac{rR_L}{r+R_L(1-D)^2}, \quad (2.103)$$

the gain Z_{ox} is

$$Z_{ox} = \frac{R_L r_C}{R_L+r_C}, \quad (2.104)$$

and the angular frequency of the left-half plane zero ω_{rl} is

$$\omega_{rl} = \frac{r}{L}. \quad (2.105)$$

The angular frequency of the left-half plane zero ω_{zn} is given in (2.34). Fig. 2.18 shows the theoretically obtained magnitude and phase plots of the output impedance. The

theoretical results were validated by simulation. Fig. 2.19 shows the magnitude and phase plots of the output impedance using SABER Simulator. The output impedance at dc is approximately equal to $Z_o(0) = R_o = 0.2\ \Omega$. At dc, the inductor is a short-circuit and the filter capacitor is an open-circuit. The dc resistance is due to the parallel combination of the load resistance R_L and the equivalent series resistance r. With increase in frequency, the capacitive reactance is high and the reactance is mostly offered by the inductive reactance. At a frequency f_o, the inductive and capacitive reactances are equal and the converter filter network undergoes resonance. Beyond f_o, the capacitive reactance dominates and reduces the output impedance to nearly zero. A positive increase in the load current causes an increase in the output voltage in the negative direction causing a phase difference of $-180°$ at dc and low frequencies. Summary of calculated values for open-loop transfer functions are given in Table 2.2.

2.6 Inner-Current Loop

Fig. 2.20 shows the architecture of the inner-current loop with filter. Fig. 2.21 shows the circuit of buck-boost dc-dc converter with inner-current loop. A sense resistor R_s is placed in the inductor branch to sense the inductor current and is a part of the feedback network. At low duty ratios, the sensed inductor current ripple is high. Therefore, the control voltage intersects with the modulator ramp voltage twice in each cycle resulting in subharmonic instability. The low-pass filter attenuates the switching frequency components and its harmonics present in the sensed voltage $v_{RS} = R_s i_L$. Therefore, the theoretically obtained output voltage of the low-pass filter is $V_{FI} = R_s I_L$ and is governed by the dc component of the sensed inductor current. Thus, in this method the *true-average* component of the inductor current is sensed, thereby reducing the problems due to subharmonic instability and transistor misgating. The transfer functions related to the inner-current loop, which includes

Table 2.2: Summary of calculated values for open-loop transfer functions

Variable	**Value**
$\|T_{po}\|$	$22.63 = 27.1$ dB
$\|T_{pio}\|$	$25.13 = 18.05$ dB
$\|M_{vo}\|$	$0.438 = -7.2$ dB
$\|M_{vio}\|$	$0.2582 = -11.8$ dB
$\|Z_{io}\|$	$12.05 = 21.6$ dB
$\|Z_{oo}\|$	$0.187 = -14.6$ dB
ω_o	20.33 krad/s
f_o	3.24 kHz
ξ	0.3214
ω_{zi}	4.38 krad/s
f_{zi}	697 Hz
ω_{zvi}	3.32 krad/s
f_{zvi}	528.4 Hz
ω_{zn}	833.3 krad/s
f_{zn}	132.63 kHz
ω_{zp}	382.2 krad/s
f_{zp}	60.83 kHz
ω_{rl}	9.29 krad/s
f_{rl}	1.48 kHz

filter in the feedback path are derived and discussed in the following sections.

2.6.1 Design

The steady-state average inductor current is $I_L = V_O/[R_L(1-D)] = 2.947$ A. At a duty cycle $D = 0.3213$ and assuming the peak sawtooth voltage of the pulse-width

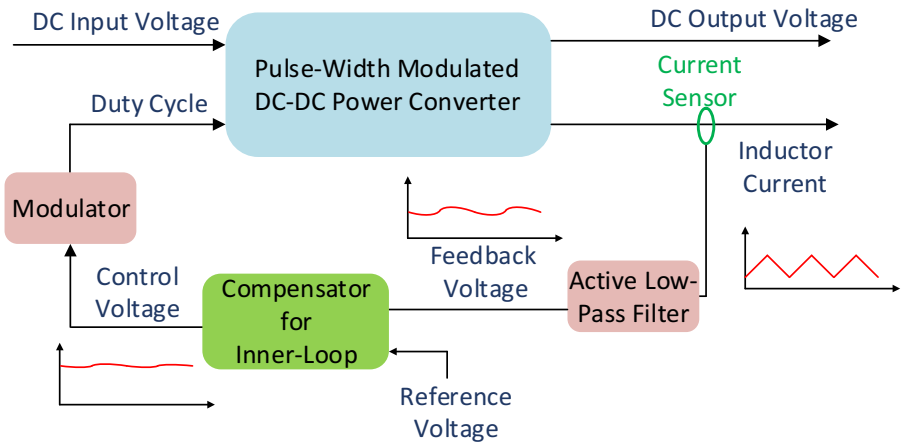

Figure 2.20: Architecture of the inner-current loop with filter block.

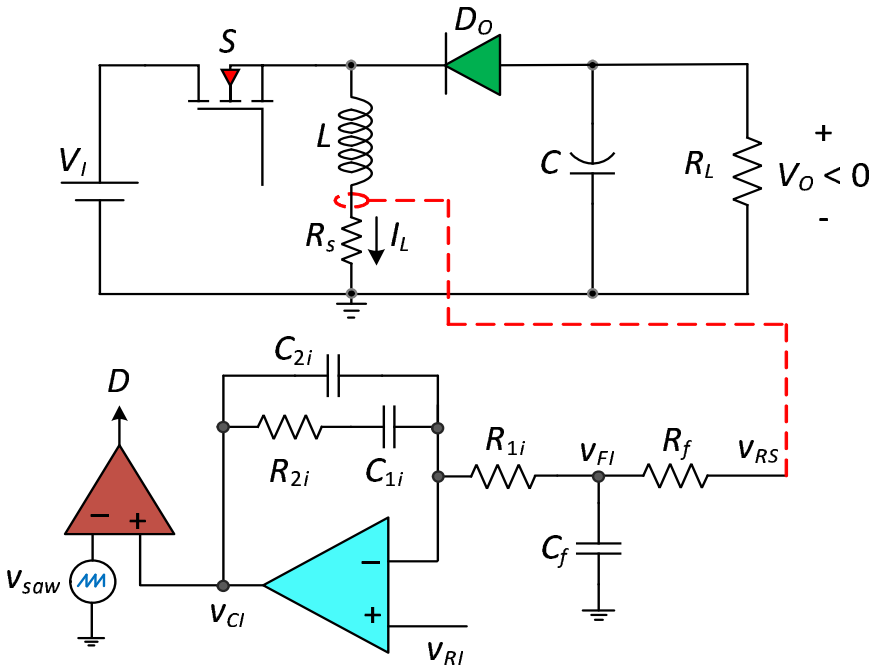

Figure 2.21: Circuit of buck-boost dc-dc converter with inner-current loop.

modulator is $V_{Tm} = 5$ V, the required steady-state control voltage is $V_{CI} = DV_{Tm} = 0.3213 \times 5 = 1.61$ V. The reference voltage to the current-loop is $V_{RI} = V_{CI}$ at steady-state since the error voltage is zero, i.e., $V_{RI} = 1.61\ V$. The gain of the feedback path is controlled mainly by the sensor gain R_s such that $Tpicl \approx 1/Rs$. For a steady-state inductor current I_L and the inner-loop reference voltage V_{RI}, which is assumed to be

set by the outer voltage loop, the sense resistor can be determined using

$$R_s = \frac{V_{Rs}}{I_L} = \frac{V_{RI}}{I_L} = \frac{1.61}{2.947} = 0.5452\ \Omega. \tag{2.106}$$

A standard resistor $R_s = 0.5\ \Omega$ was chosen.

2.6.2 Transfer Function of Filter T_f

The low-pass filter stage is composed of a resistor R_f and a capacitor C_f, placed in series with the non-inverting amplifier. The transfer function of two stages is

$$\begin{aligned} T_f(s) = \frac{v_{fi}(s)}{v_{rs}(s)} &= \frac{Z_{Cf}}{Z_{Cf} + R_f} = \frac{\frac{1}{sC_f}}{\frac{1}{sC_f} + R_f} = \frac{1}{1 + sR_fC_f} \\ &= \frac{1}{R_fC_f}\frac{1}{s + \frac{1}{R_fC_f}} = \frac{\omega_{pf}}{s + \omega_{pf}} = \frac{1}{\frac{s}{\omega_{pf}} + 1}. \end{aligned} \tag{2.107}$$

$$T_f(s) = \frac{1}{\frac{j\omega}{\omega_{pf}} + 1}, \tag{2.108}$$

where

$$f_{pf} = \frac{\omega_{pf}}{2\pi} = \frac{1}{2\pi R_fC_f}. \tag{2.109}$$

Rearranging

$$T_f\left(\frac{j\omega + \omega_{pf}}{\omega_{pf}}\right) = 1 \tag{2.110}$$

$$T_f(j\omega + \omega_{pf}) = \omega_{pf}. \tag{2.111}$$

Further modification results in

$$\omega_{pf} = \frac{jT_f\omega}{1 - T_f} \tag{2.112}$$

and hence

$$f_{pf} = \frac{jT_ff}{1 - T_f}. \tag{2.113}$$

Therefore, the filter upper cutoff frequency can be obtained as

$$f_{pf} = \frac{T_f f}{1 - T_f}. \tag{2.114}$$

The filter frequency can be set by the amount of attenuation desired. For an example, to achieve an attenuation of 33% in the filter output voltage at the switching frequency, i.e., $|T_f|(f_s) = 0.33$, the filter upper cutoff frequency using (2.114) must be $f_{pf} = 0.5 f_s = 100$ kHz. Using (2.109), for $f_{pf} = 100$ kHz and $R_f = 1$ kΩ, $C_f = 1.6$ nF.

2.6.3 Transfer Function of Pulse-Width Modulator T_m

The control voltage-to-duty cycle transfer function of the pulse-width modulator is

$$T_m = \frac{D}{V_C} = \frac{d}{v_c} = \frac{1}{V_{Tm}}, \tag{2.115}$$

where V_{Tm} is the amplitude of the sawtooth waveform. For $V_{Tm} = 5$ V, $T_m = 0.2$ 1/V.

2.6.4 Uncompensated Loop Gain T_{ki}

The natural behavior of the inner-current loop can be determined using the uncompensated loop gain as

$$T_{ki} = \frac{v_{fi}}{v_{ei}} = T_m T_{pi} R_s T_f = T_{ki0} \frac{1 + \frac{s}{\omega_{zi}}}{\left(1 + \frac{s}{\omega_{pf}}\right)\left(1 + \frac{2\xi s}{\omega_0} + \frac{s^2}{\omega_0^2}\right)}, \tag{2.116}$$

where T_m, T_{pi}, and T_f are given in (2.115), (2.41), and (2.107), respectively. The dc gain T_{ki0} is given by

$$T_{ki0} = \frac{R_s}{V_{Tm}} \frac{V_I + 2V_O}{r + R_L(1 - D)^2}. \tag{2.117}$$

Fig. 2.22 shows the theoretically obtained magnitude and phase plots of the uncompensated loop gain of the inner-current loop. The gain at dc is $T_{ki0} = 5.88$ dB = 1.97 V/V. A high dc gain T_{ki0} is required in view of the reducing the steady-state error in the output voltage due ti step changes in the input voltage or load current. Therefore, a suitable control circuit capable of providing a high gain at dc and provide

sufficient phase boost at the crossover frequency of the loop gain becomes essential. An important factor to note is that the phase of the uncompensated loop gain is zero at dc. This is because the inner-loop absorbs only the inductor branch and does not take into account the properties of the output network. Typically, the presence of a low-frequency zero in the T_{pi} transfer function enables a wider current loop bandwidth and low phase at the crossover frequency. The phase margin is in the range 40° to 90° and requires relatively simpler compensation schemes to satisfy the inner current loop requirements. In this work, the Type-II integral control circuit (also known as the single-lead integral control circuit) is used.

2.6.5 Transfer Function of Compensation Circuit T_{ci}

An integral-single-lead control circuit introduces a pole at the origin required to boost the dc gain and a pole-zero pair to adjust crossover frequency f_c to maintain required PM. A detailed procedure to determine the transfer function of the controller to

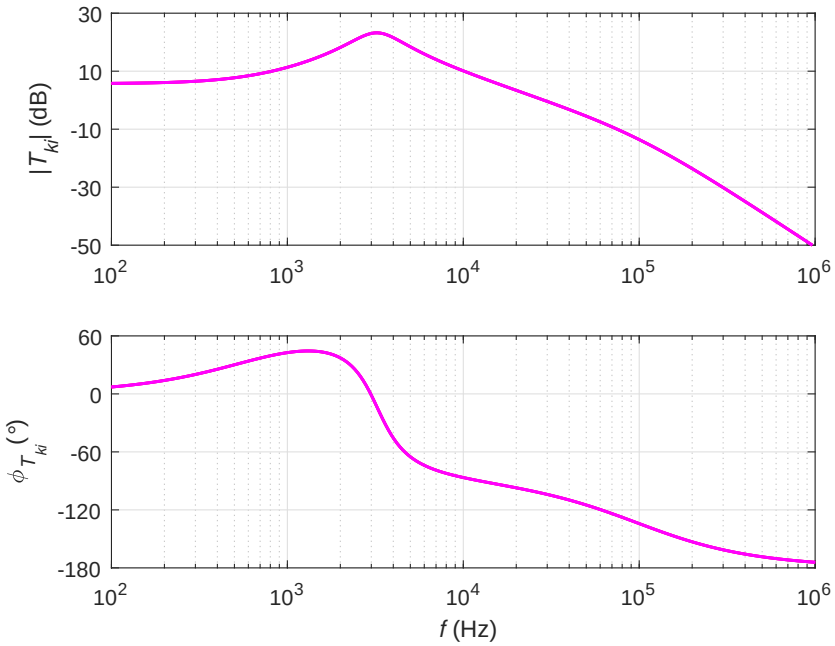

Figure 2.22: Theoretically obtained magnitude and phase plots of the uncompensated loop gain T_{ki} of inner-current loop.

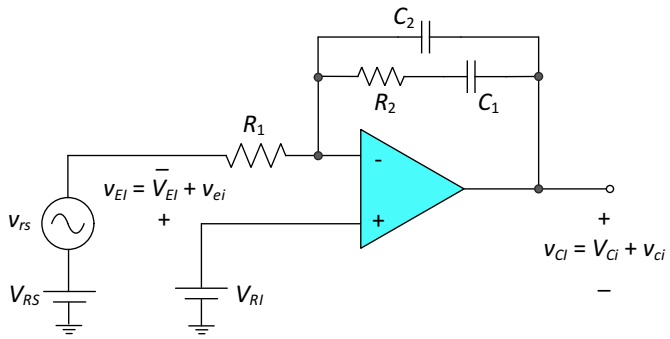

Figure 2.23: Circuit of type-II compensator.

improve the dc gain ($>$ 50 dB) and achieve an inner-current loop phase margin $PM = 60°$ is explained in [34].The design can be performed as follows. The magnitude of the uncompensated loop gain transfer function can be determined using

$$|T_{ki}(f)| = T_{ki0}\frac{\sqrt{1+\left(\frac{f}{f_{zi}}\right)^2}}{\sqrt{1+\left(\frac{f}{f_{ff}}\right)^2}\sqrt{1-\left(\frac{f}{f_0}\right)^2+(4\xi^2\left(\frac{f}{f_0}\right)^2}} \tag{2.118}$$

and the phase is

$$\phi_{Tk}(f) = -180° + \tan^{-1}\left(\frac{f}{f_{zi}}\right) - \tan^{-1}\left(\frac{f}{f_{ff}}\right) - \tan^{-1}\frac{2\xi\frac{f}{f_0}}{1-\left(\frac{f}{f_0}\right)^2}. \tag{2.119}$$

The desired crossover frequency for the loop gain is chosen as $f_c = 30$ kHz. At this frequency, the magnitude of the uncompensated loop gain transfer function is $|T_{ki}(f_c)| = -0.536$ dB $= 0.94$ and its phase is $\phi_{Tk}(f_c) = -104°$. The required phase margin is $PM = 60°$. Therefore, the phase boost required at f_c is

$$\phi_m = M - \phi_{Tk}(f_c) - 90° = 74.0196°, \tag{2.120}$$

giving the geometric mean between the compensator corner frequencies as

$$K = \tan^{-1}\left(\frac{\phi_m}{2} + 45°\right) = 7.124. \tag{2.121}$$

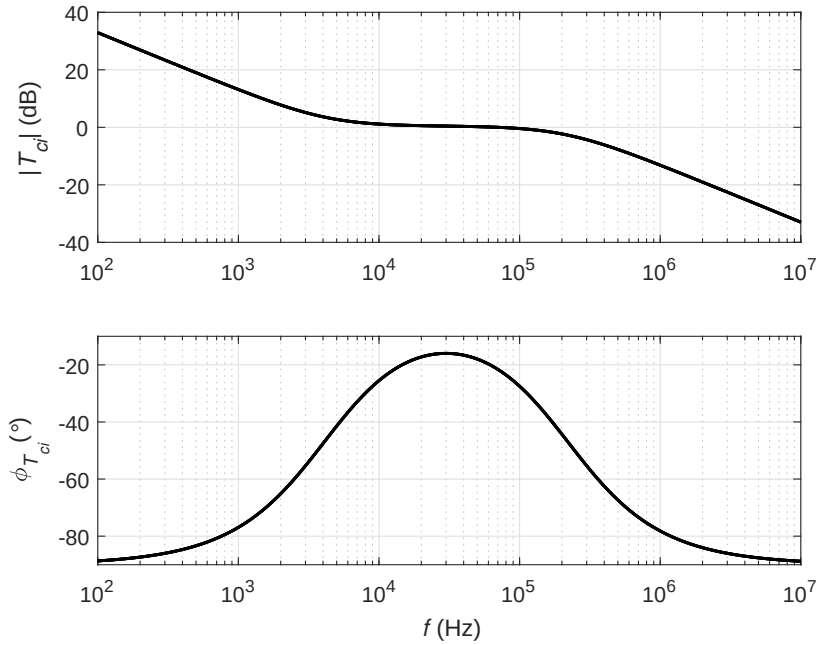

Figure 2.24: Theoretically obtained magnitude and phase plots of controller transfer function T_{ci} for the inner-current loop.

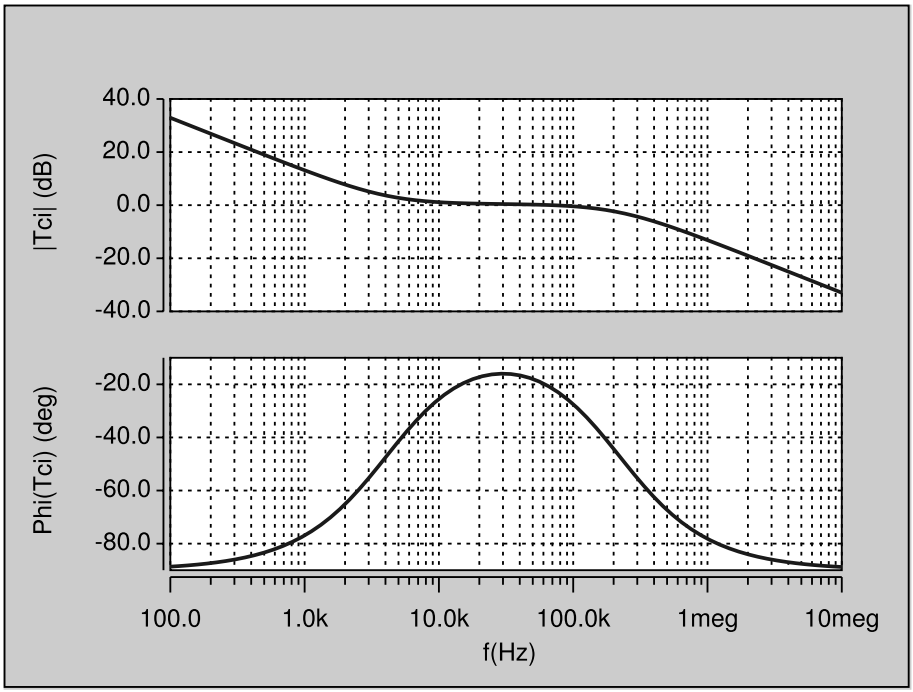

Figure 2.25: Magnitude and phase plots of output impedance obtained by circuit simulation of controller transfer function T_{ci} for the inner-current loop.

Assuming $R_1 = 1$ kΩ, the value of C_2 is

$$C_2 = \frac{|T_k(f_c)|}{2\pi f_c K R_1} = 708.96 \text{ pF}. \tag{2.122}$$

The expression for C_1 is

$$C_1 = C_2(K^2 - 1) = 35.27 \text{ nF}. \tag{2.123}$$

The expression for R_2 is

$$R_2 = \frac{K}{2\pi f_c C_1} = 1.07 \text{ k}\Omega. \tag{2.124}$$

The transfer function T_{ci} of the current loop control circuit is

$$T_{ci}(s) = \frac{v_{ci}(s)}{v_{ei}(s)} = T_{cio}\frac{1 + \dfrac{s}{\omega_{zci}}}{s\left(1 + \dfrac{s}{\omega_{pci}}\right)}, \tag{2.125}$$

where

$$T_{cio} = \frac{1}{R_1(C_1 + C_2)}, \tag{2.126}$$

$$\omega_{zci} = \frac{1}{R_2 C_1}, \tag{2.127}$$

and

$$\omega_{pci} = \frac{C_1 + C_2}{R_2 C_1 C_2}. \tag{2.128}$$

Fig. 2.24 shows the theoretically obtained magnitude and phase plots of the compensator transfer function used in the inner-current loop. The theoretical results were validated by simulation. Fig. 2.25 shows the magnitude and phase plots of the compensator transfer function used in the inner-current loop using SABER Simulator. The control transfer function is now incorporated into the critical path to determine the inner-loop gain and is discussed in the following section.

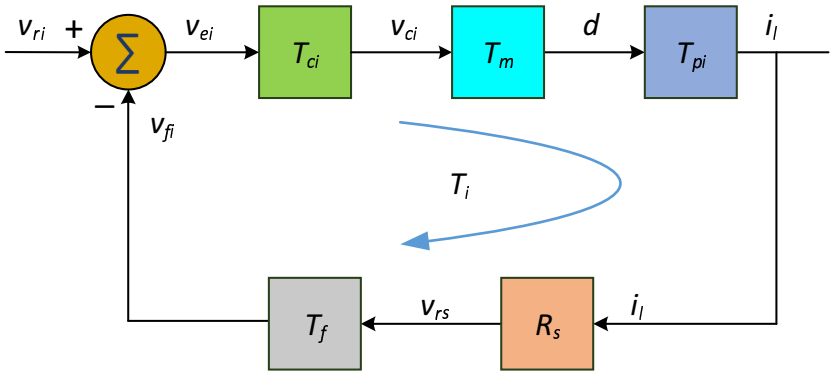

Figure 2.26: Block diagram of inner-current loop.

2.6.6 Compensated Loop Gain T_i

The loop gain of the compensated inner-current loop is

$$T_i = \frac{v_{ei}}{v_{fi}} = T_{ki}T_{ci} = T_m T_{pi} R_s T_f T_{ci}, \tag{2.129}$$

to yield

$$T_i = T_{i0} \frac{\left(1 + \frac{s}{\omega_{zi}}\right)\left(1 + \frac{s}{\omega_{zci}}\right)}{s\left(1 + \frac{s}{\omega_{pf}}\right)\left(1 + \frac{s}{\omega_{pci}}\right)\left(1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}\right)}, \tag{2.130}$$

where T_{i0} is the gain at $s = 0$ given as

$$T_{i0} = T_{ki0}T_{ci0} = \frac{V_I R_s}{V_{Tm}(R_L + r)} \frac{1}{R_1(C_1 + C_2)}. \tag{2.131}$$

Fig. 2.27 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop. The theoretical results were validated by simulation. Fig. 2.28 shows the magnitude and phase plots of compensated loop gain of the inner-current loop using SABER Simulator. The gain at dc is greater than 50 dB and the phase at dc starts at 90° due to the presence of controller pole at origin. The unity gain crossover frequency is 30 kHz and the phase margin is $PM = 60°$. The inner-loop is stable. The following section describes the various important closed-loop transfer functions of the inner-current loop.

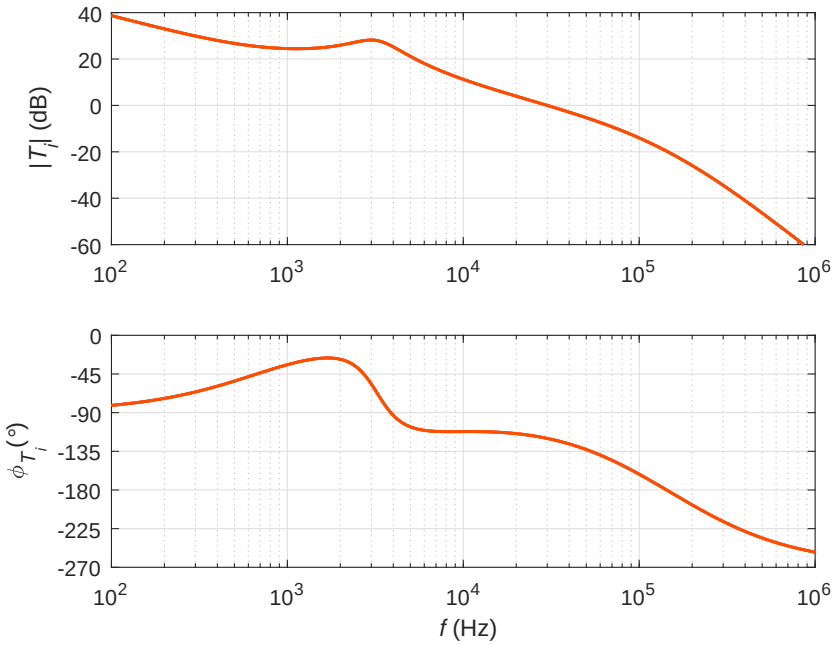

Figure 2.27: Theoretically obtained magnitude and phase plots of compensated loop gain T_i of the inner-current loop.

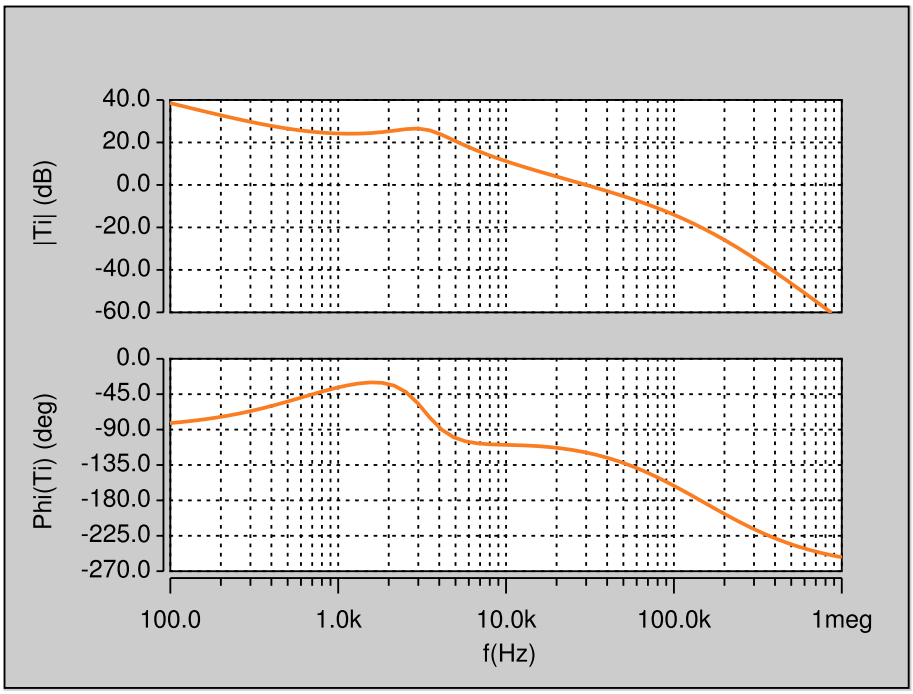

Figure 2.28: Magnitude and phase plots of compensated loop gain T_i of the inner-current loop obtained by circuit simulation.

2.7 Closed-Inner Loop Transfer Functions

The following closed-loop transfer functions relevant to the inner-loop are derived:

- Reference voltage to inductor current transfer function T_{icl} (Control).
- Reference voltage to output voltage transfer function T_{picl} (Control).
- Input voltage-to-inductor current transfer function M_{icl} (Disturbance).
- Input voltage-to-output voltage transfer function M_{vicl} (Disturbance).
- Input voltage-to-duty cycle transfer function M_{di} (Disturbance).
- Input Impedance Z_{iicl} (Disturbance).
- Output Impedance Z_{oicl} (Disturbance).

The block diagram required to characterize the inner current loop is as shown in Fig. 2.29. The small-signal current reference v_{ri} to the inner-loop is set by the outer loop. The focus of this section is to analyze the inner-current loop only. Therefore, the outer-voltage loop has not been shown in the block diagram. The error voltage v_{ei} is formed by the difference between the current reference v_{ri} and the feedback voltage v_{fi}. The feedback voltage v_{fi} is given by

$$v_{fi} = T_f R_s i_l, \tag{2.132}$$

where T_f is the transfer function of the low-pass filter and R_s is the sense resistor. The transfer function T_f is given by

$$T_f = \frac{v_{fi}}{v_{rs}} = \frac{1}{1 + \dfrac{s}{\omega_{ff}}}, \tag{2.133}$$

where $\omega_{ff} = 2\pi f_{ff}$ is the filter cutoff frequency. In this work, the filter cutoff frequency is selected as $0.5 f_s$ and is based on the allowable ripple in the sensed inductor

current contributing the concept of the true-average current-mode control (explained in Section 2.6.2). The gain of the low-pass filter is unity, therefore, it does not affect the dc gain of the loop gain. The transfer function T_{ci} is the voltage gain of the Type-II control circuit mentioned in the previous sections. The pulse-width modulator has a linear gain $T_m = 1/V_{Tm}$, where V_{Tm} is the maximum value of the sawtooth waveform.

As the inductor current is controlled by the inner-loop, the inductor current must be sensed, amplified by R_s, filtered by T_f, and compared to current reference v_{ri} to generate the small-signal error. The following sections perform a complete characterization of the inner current loop.

2.7.1 Reference Voltage-to-Inductor Current Transfer Function T_{icl}

Using the block diagram shown in Fig. 2.29, the closed-loop reference voltage-to-inductor current transfer function is

$$T_{icl}(s) = \left.\frac{i_l(s)}{v_{ri}(s)}\right|_{v_i=i_o=0}. \tag{2.134}$$

From Fig. 2.29

$$i_l = T_{ci}T_mT_{pi}v_{ei}, \tag{2.135}$$

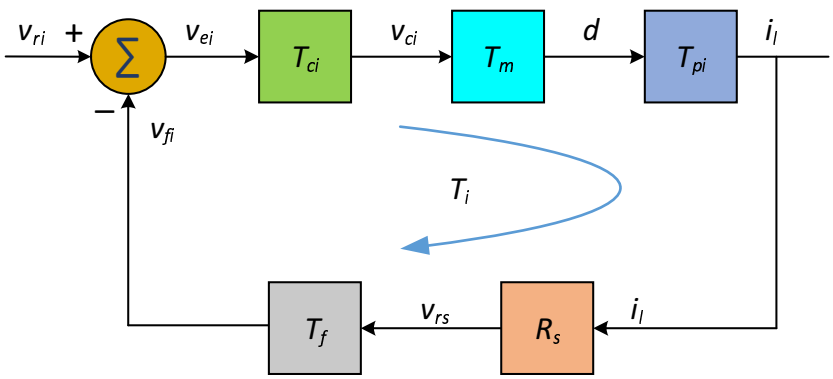

Figure 2.29: Block diagram used to derive inner-loop control-to-inductor current transfer function T_{icl}.

hence

$$v_{ei} = \frac{i_l}{T_{ci} T_m T_{pi}} \tag{2.136}$$

and

$$v_{fi} = T_f R_s i_l. \tag{2.137}$$

Also, the error voltage is

$$\begin{aligned} v_{ei} &= v_{ri} - v_{fi}. \\ v_{ri} &= v_{ei} + v_{fi}. \end{aligned} \tag{2.138}$$

Substituting (2.136) and (2.137) in (2.138), we get

$$\begin{aligned} v_{ri} = v_{ei} + v_{fi} &= \frac{i_l}{T_{ci} T_m T_{pi}} + T_f R_s i_l = \left(\frac{1}{T_{ci} T_m T_{pi}} + T_f R_s \right) i_l \\ &= \left(\frac{1 + T_{ci} T_m T_{pi} T_f R_s}{T_{ci} T_m T_{pi}} \right) i_l = \left(\frac{1 + T_i}{T_{ci} T_m T_{pi}} \right) i_l \end{aligned} \tag{2.139}$$

$$T_{icl}(s) = \left. \frac{i_l(s)}{v_{ri}(s)} \right|_{v_i = i_o = 0} = \frac{T_{ci} T_m T_{pi}}{1 + T_i}. \tag{2.140}$$

Fig. 2.30 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop reference voltage-to-inductor current transfer function. The theoretical results were validated by simulation. Fig. 2.31 shows the magnitude and phase plots of the inner-current loop reference voltage-to-inductor current transfer function using SABER Simulator. It can be observed that the bandwidth of the current loop seen by T_{icl} is high and equal to nearly 40 kHz. There is still a margin for bandwidth improvement but at the cost of reduced dc gain. The transfer function T_{icl} does not encompass the transfer function T_p (i.e., relevant to the outer voltage loop). Therefore, maximum speed can be achieved by the inner current loop itself. This means that for any input or load disturbance, the inner-loop alone can sufficiently counteract the disturbance and provide the necessary correction in the inductor current. Ideally, the inductor current is made to follow the fixed current reference v_{ri}, therefore, this form of the current-mode control can also be referred to as *current programmed control*.

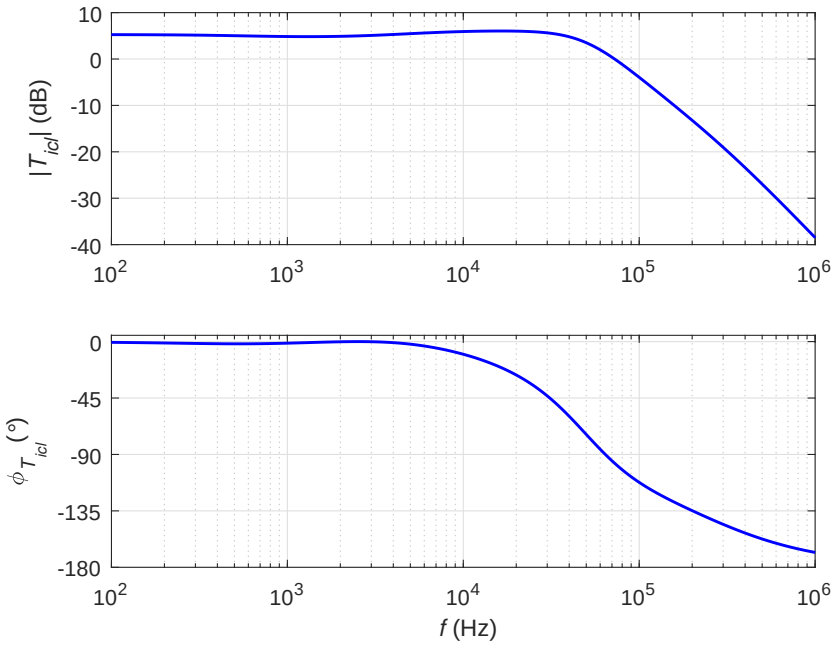

Figure 2.30: Theoretically obtained magnitude and phase plots of the inner-current loop reference voltage-to-inductor current transfer function T_{icl}.

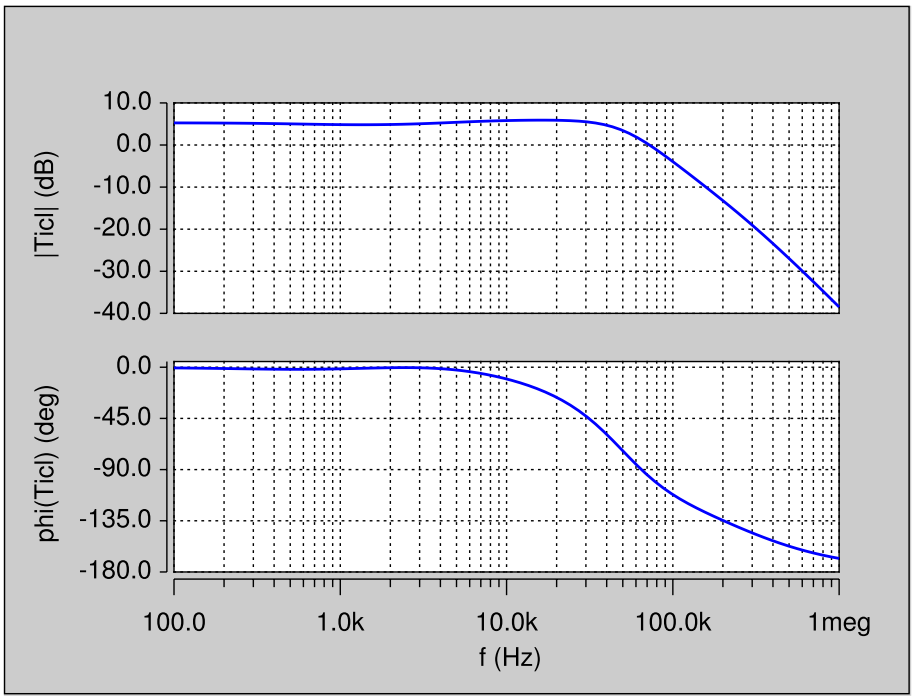

Figure 2.31: Magnitude and phase plots of the inner-current loop reference voltage-to-inductor current transfer function T_{icl} obtained by circuit simulation.

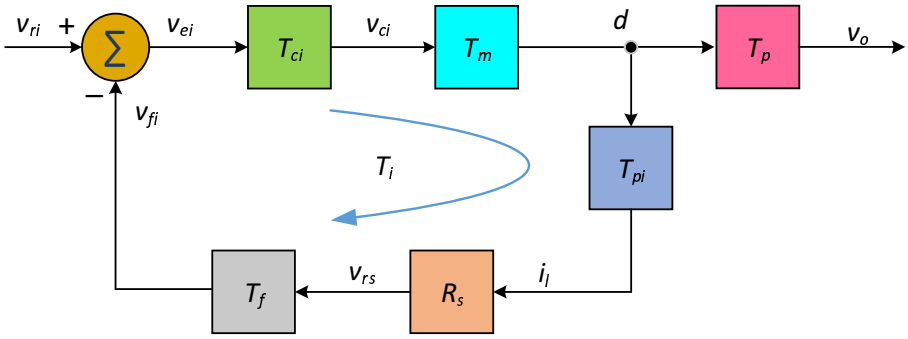

Figure 2.32: Block diagram required to derive inner-loop control-to-output voltage transfer function T_{picl}.

The following approximation of (3.14) holds true as the loop gain $T_i >> 1$

$$T_{icl} = \frac{T_{ci}T_mT_{pi}}{1 + T_mT_{ci}T_{pi}T_fR_s} \approx \frac{T_{ci}T_mT_{pi}}{T_mT_{ci}T_{pi}T_fR_s} = \frac{1}{T_fR_s}. \tag{2.141}$$

2.7.2 Reference Voltage-to-Output Voltage Transfer Function T_{picl}

Using the block diagram shown in Fig. 2.32, the closed-loop reference voltage-to-output voltage transfer function is

$$T_{picl}(s) = \frac{v_o(s)}{v_{ri}(s)}\bigg|_{v_i=i_o=0} = \frac{T_{ci}T_mT_p}{1 + T_i}. \tag{2.142}$$

At low frequencies, $T_i >> 1$, therefore

$$T_{picl} \approx \frac{T_{ci}T_mT_p}{T_i} = \frac{T_p}{T_fR_s}. \tag{2.143}$$

Fig. 2.33 shows the theoretically obtained magnitude and phase plots of inner-current loop reference voltage-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 2.34 shows the magnitude and phase plots of the inner-current loop reference voltage-to-output voltage transfer function using SABER Simulator. The reference voltage and the output voltage are out of phase by 180°. The bandwidth of the loop from the reference to the output is limited due to the filter capacitor. A critical difference can be observed through the block diagram used

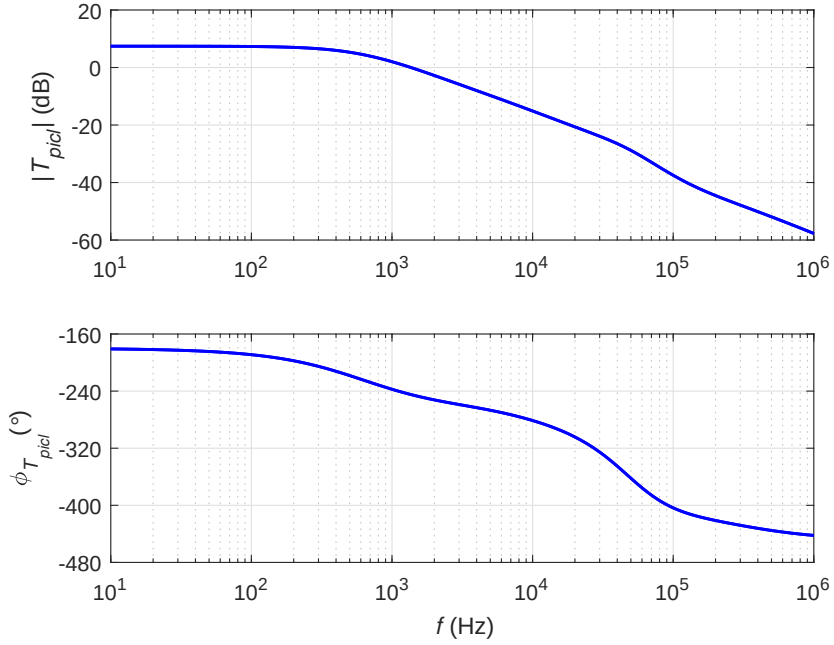

Figure 2.33: Theoretically obtained magnitude and phase plots of reference voltage-to-output voltage transfer function T_{picl}.

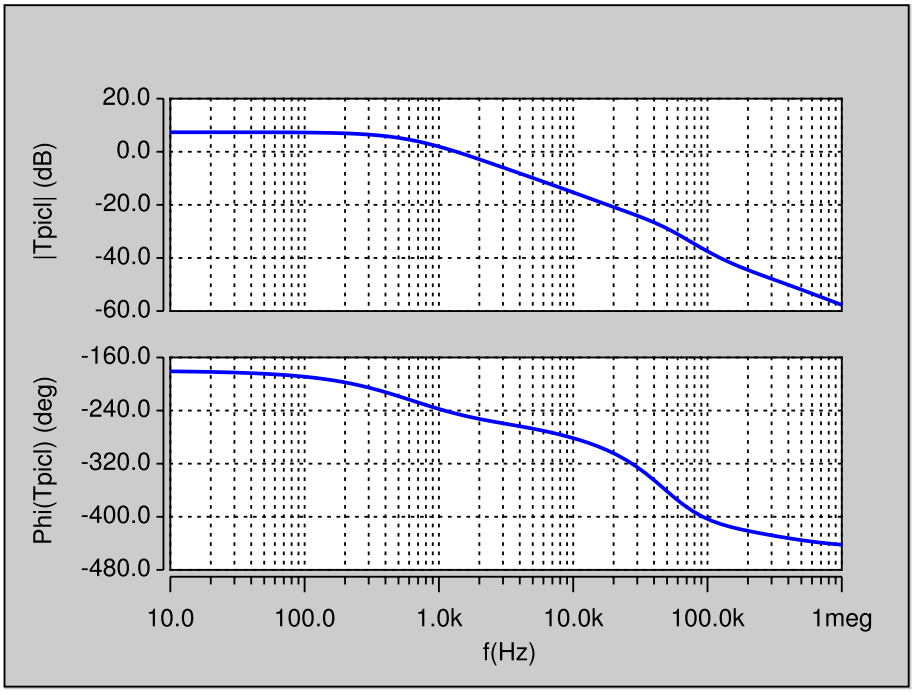

Figure 2.34: Magnitude and phase plots ofReference voltage-to-output voltage transfer function T_{picl} obtained by circuit simulation.

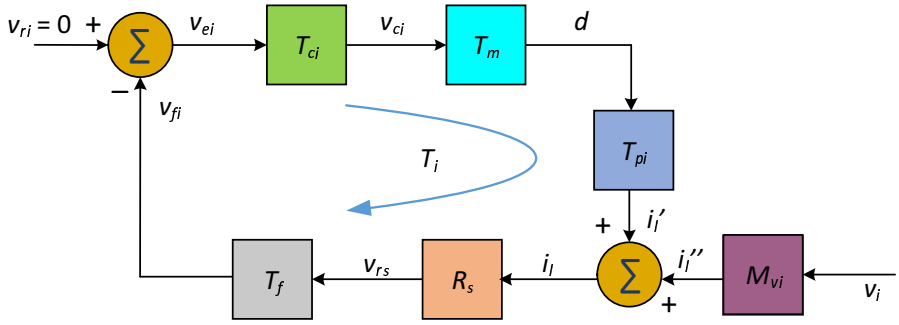

Figure 2.35: Block diagram required to derive inner-loop input voltage-to-inductor current transfer function M_{icl}.

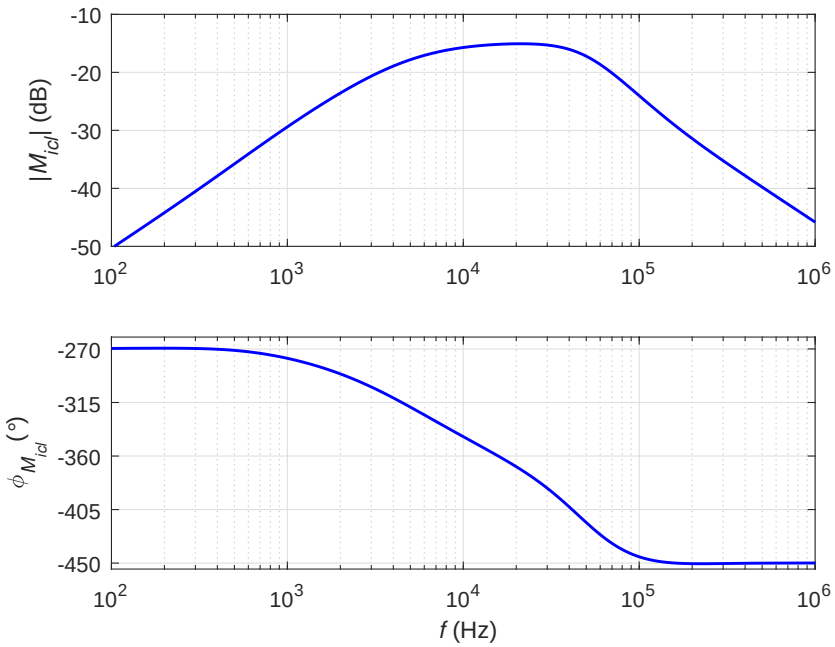

Figure 2.36: Theoretically obtained magnitude and phase plots of input voltage-to-inductor current transfer function M_{icl}.

to derive the T_{picl} transfer function. The output voltage is controlled by the duty cycle in the buck-boost converter, whereas the inductor current controls the output voltage in buck converters. In order to characterize the outer loop transfer functions such as T_{picl}, the critical path of the model is converted from voltage-controlled current source (i_l/v_{ri}) to voltage-controlled voltage source (d/v_{ri}). This aspect has not been previously reported in literature.

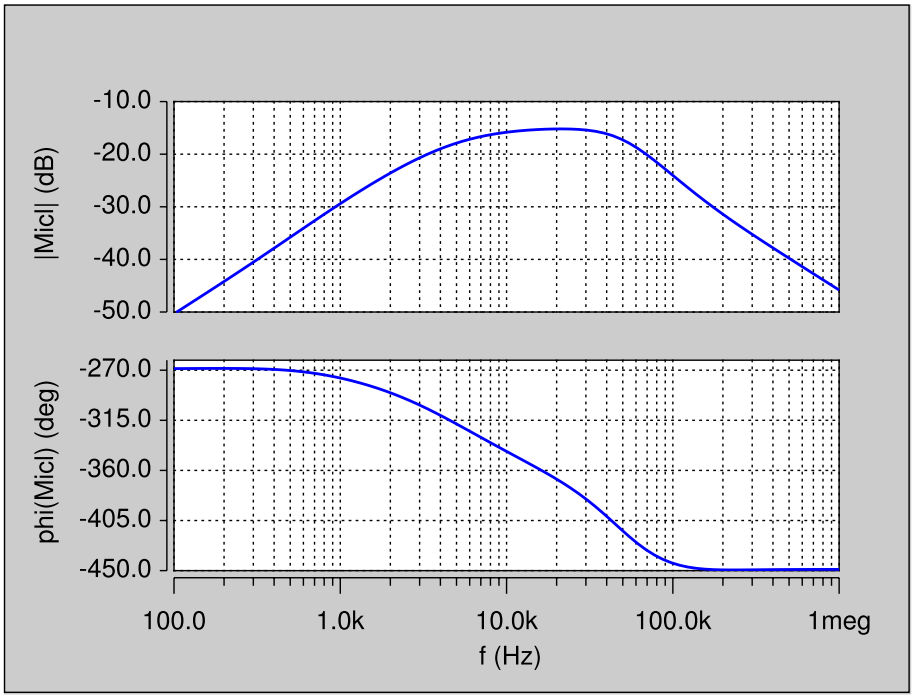

Figure 2.37: Magnitude and phase plots of input voltage-to-inductor current transfer function M_{icl} obtained by circuit simulation.

2.7.3 Input Voltage-to-Inductor Current Transfer Function M_{icl}

Using the block diagram shown in Fig. 2.35, the closed-loop input voltage to inductor current transfer function is

$$M_{icl}(s) = \left.\frac{i_l(s)}{v_i(s)}\right|_{v_{ri}=i_o=0}. \tag{2.144}$$

From the block diagram

$$i_l = i_l' + i_l'' = (-T_i)i_l + M_{vi}v_i. \tag{2.145}$$

$$i_l(1+T_i) = M_{vi}v_i. \tag{2.146}$$

Hence

$$M_{icl}(s) = \frac{i_l(s)}{v_i(s)} = \frac{M_{vi}}{1+T_i}. \tag{2.147}$$

Fig. 2.36 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop input voltage-to-inductor current transfer

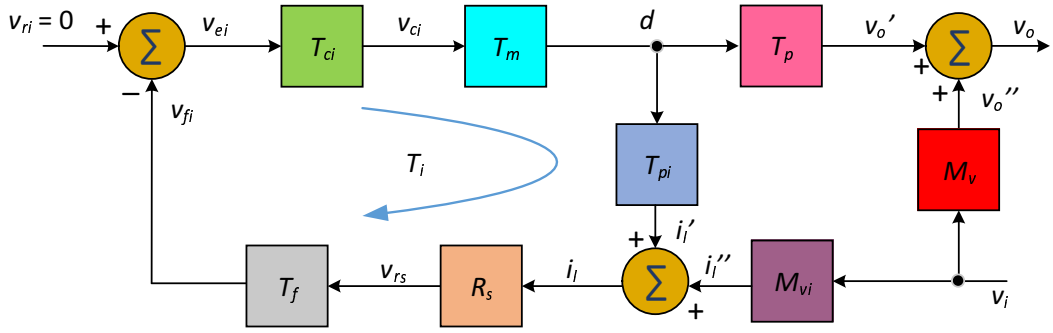

Figure 2.38: Block diagram required to derive inner-loop input voltage-to-output voltage transfer function M_{vicl}.

function. The theoretical results were validated by simulation. Fig. 2.37 shows the magnitude and phase plots of the inner-current loop input voltage-to-inductor current transfer function using SABER Simulator. As can be seen from (2.147), the M_{icl} transfer function is a representative case to show the effect of negative feedback, i.e., the negative feedback path reduces the disturbance in the input voltage to propagate through the inductor current branch by a factor of nearly T_i. However, this is possible only at low to mid frequencies and in the range of frequencies up to f_c, where $T_i >> 1$. Beyond, this frequency range $T_i << 1$ and the transfer function $M_{icl} \approx M_{vi}$. The gain at dc and low frequencies is -50 dB or lower, indicating that the inner-loop can sufficiently attenuate the input voltage disturbance. The phase starts at $-270°$ or $90°$ due to the presence the pole at origin in the loop gain transfer function T_i.

2.7.4 Input Voltage-to-Output Voltage Transfer Function M_{vicl}

Using the block diagram shown in Fig. 2.38, the closed-loop input voltage to output voltage transfer function is

$$M_{vicl}(s) = \left.\frac{v_o(s)}{v_i(s)}\right|_{v_{ri}=i_o=0}. \tag{2.148}$$

From the block diagram

$$i_l = i_l' + i_l'' = T_{pi}d + M_{vi}v_i \tag{2.149}$$

and

$$\frac{-d}{T_{ix}} = T_{pi}d + M_{vi}v_i, \tag{2.150}$$

where

$$T_{ix} = \frac{T_i}{T_{pi}} = T_{ci}T_m R_s T_f. \tag{2.151}$$

Rearranging

$$-d\left(\frac{1}{T_{ix}} + T_{pi}\right) = M_{vi}v_i. \tag{2.152}$$

$$-d\left(\frac{1 + T_{ix}T_{pi}}{T_{ix}}\right) = M_{vi}v_i. \tag{2.153}$$

$$d = -\frac{M_{vi}T_{ix}}{1 + T_i}v_i. \tag{2.154}$$

From the block diagram in Fig. (2.38)

$$v_o = v_o' + v_o'' = T_p d + M_v v_i. \tag{2.155}$$

Substituting d from (2.154), we get

$$v_o = T_p\left(-\frac{M_{vi}T_{ix}}{1 + T_i}v_i\right) + M_v v_i. = \left(M_v - \frac{T_p M_{vi}T_{ix}}{1 + T_i}\right)v_i. \tag{2.156}$$

The closed-loop input-to-output transfer function is

$$M_{vicl}(s) = \frac{v_o(s)}{v_i(s)} = M_v - \frac{T_p M_{vi}T_{ix}}{1 + T_i}. \tag{2.157}$$

Fig. 2.39 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop input voltage-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 2.40 shows the magnitude and phase plots of the inner-current loop input voltage-to-output voltage transfer function using SABER Simulator. The M_{vicl} transfer function is an important transfer function relevant, especially for the output voltage loop. At low frequencies, the transfer function can be approximated as follows. At low frequencies, $T_i >> 1$ to give

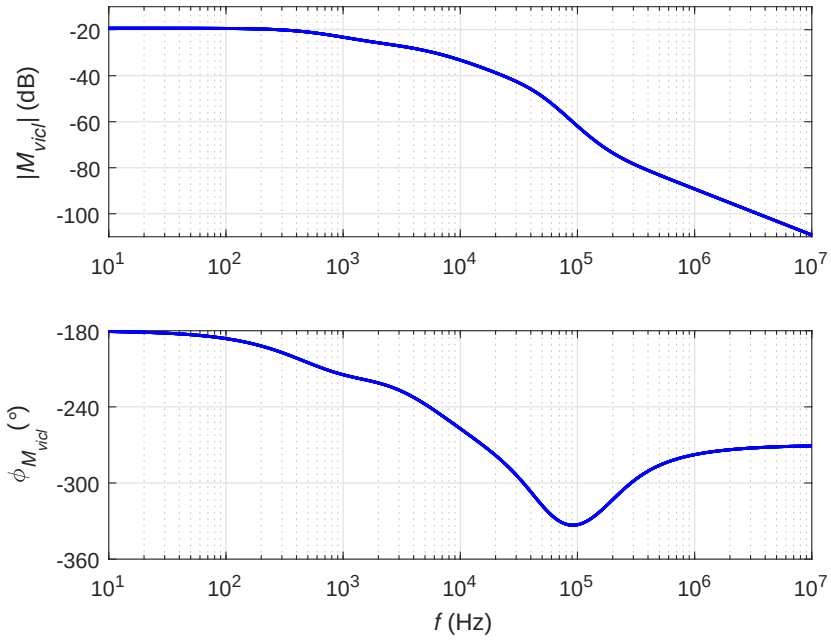

Figure 2.39: Theoretically obtained magnitude and phase plots of input voltage-to-output voltage transfer function transfer function M_{vicl}.

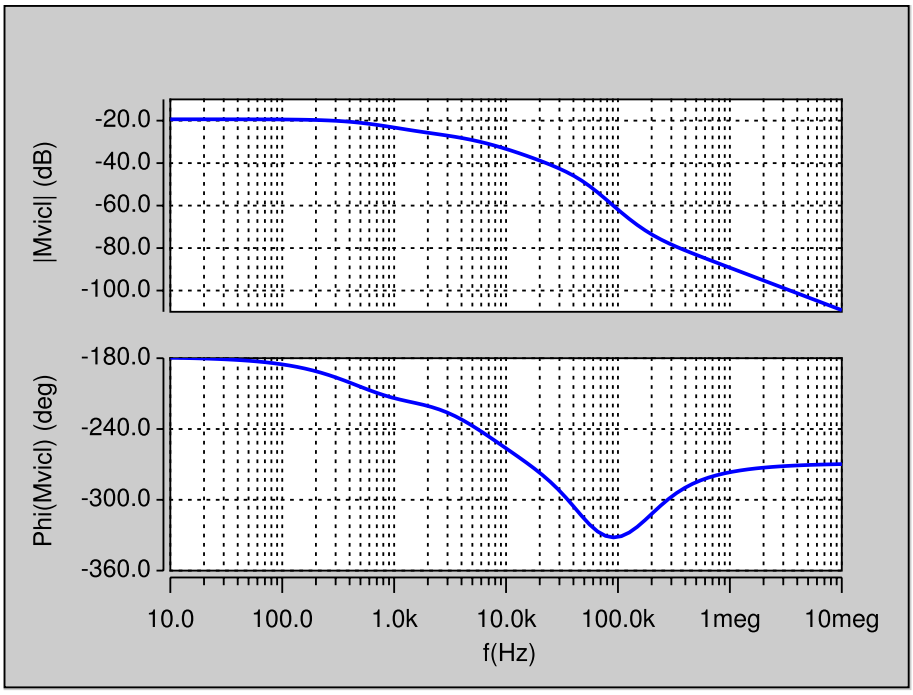

Figure 2.40: Magnitude and phase plots of input voltage-to-output voltage transfer function transfer function M_{vicl} obtained by circuit simulation.

$$M_{vicl} = M_v - \frac{T_p M_{vi} T_{ix}}{T_i} = M_v - \frac{T_p M_{vi}}{T_{pi}}. \tag{2.158}$$

Unlike other disturbance transfer functions, the M_{vicl} transfer function obtained between the output and the input in presence of the inner-current loop only depends on T_i instead of $1/T_i$. From Table 2.2, $M_{vo} = 0.438, T_{po} = 22.63, T_{pio} = 25.13$, and $M_{vio} = 0.2582$. Therefore, at dc and low frequencies, assuming $T_{io} \approx 100$, then $M_{viclo} \approx 0.206 = -13.3$ dB. Therefore, one can see that the inner current loop cannot provide large attenuation for the disturbance in input voltage from propagating to the output. However, by comparing M_{iclo} and M_{viclo}, for a disturbance in the input voltage, the amount of attenuation provided for inductor current change is much larger than that provided for the output voltage change.

2.7.5 Input Voltage-to-Duty Cycle Transfer Function M_{di}

Using the block diagram shown in Fig. 2.38, the closed-loop input voltage to duty cycle transfer function is

$$M_{di}(s) = \left.\frac{d(s)}{v_i(s)}\right|_{v_{ri}=i_o=0}. \tag{2.159}$$

From (2.154)

$$d = -\frac{M_{vi} T_{ix}}{1 + T_i} v_i. \tag{2.160}$$

Hence, the closed-loop input voltage to duty cycle transfer function is

$$M_{di}(s) = \frac{d(s)}{v_i(s)} = -\frac{M_{vi} T_{ix}}{1 + T_i} = -\frac{M_{vi}}{T_{pi}} \frac{T_i}{1 + T_i}. \tag{2.161}$$

Fig. 2.41 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop input voltage-to-control transfer function. The theoretical results were validated by simulation. Fig. 2.42 shows the magnitude and phase plots of the inner-current loop input voltage-to-control transfer function using SABER Simulator. This transfer function is critical in view of comparing

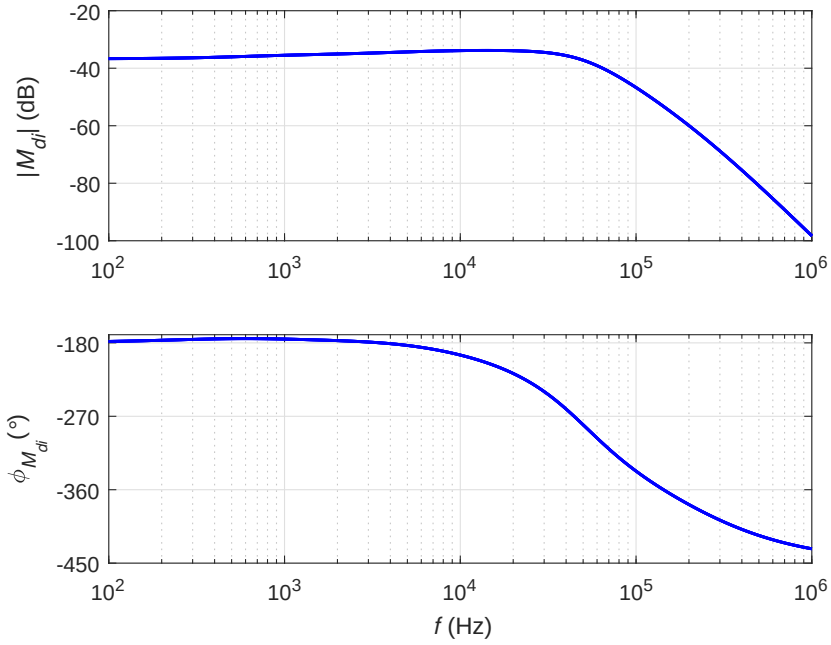

Figure 2.41: Theoretically obtained magnitude and phase plots of input voltage-to-duty cycle transfer function M_{di}.

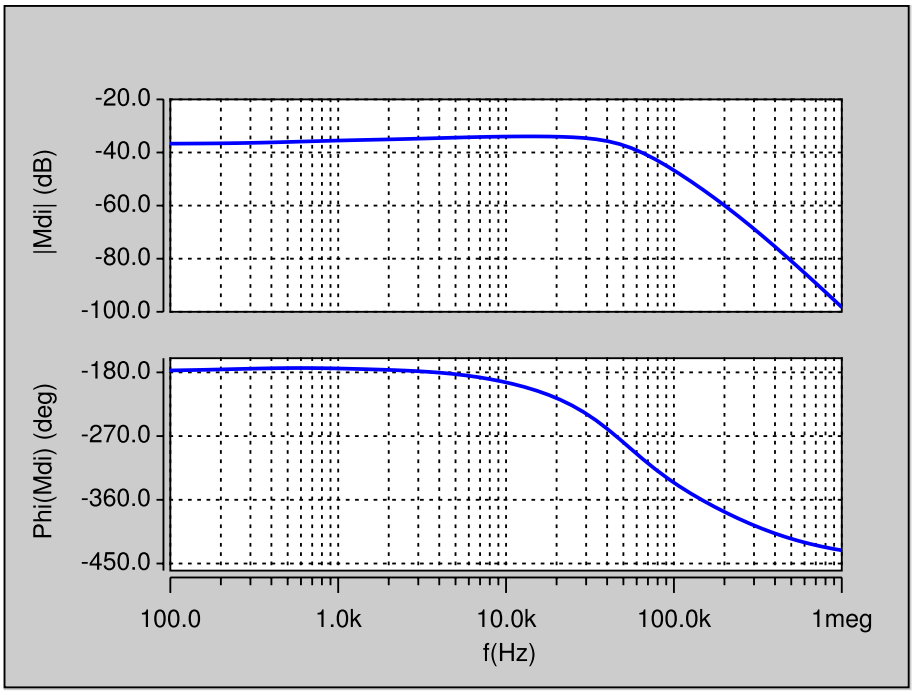

Figure 2.42: Magnitude and phase plots of input voltage-to-duty cycle transfer function M_{di} obtained by circuit simulation.

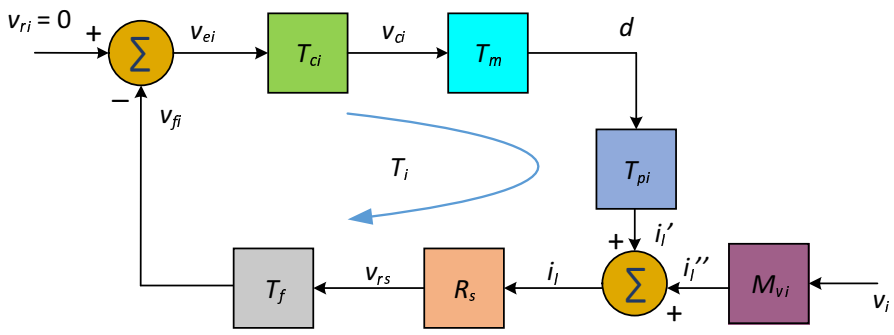

Figure 2.43: Block diagram used to derive inner-closed loop input impeance Z_{iicl}.

the magnitude of correction capable of being provided for the duty cycle by the inner-loop and the outer loop for disturbances in the input voltage. This analysis is being reported for the first time in form of transfer functions. From the Bode plot, the magnitude of the transfer function at dc is nearly $M_{di0} = 0.012$, i.e., for a step change in input voltage by 1 V, the duty cycle changes by nearly 0.012 units in order to correct the disturbance. For example, assume that the steady-state input voltage of the designed buck-boost converter changes from 12 V to 14 V, then the corresponding change in the duty cycle needed to maintain the output voltage V_O constant is $\Delta D = 0.0309$. However, the current loop is able to provide only $\Delta D = M_{di0} \times \Delta V_I = 0.012 \times 2 = 0.024$ units. This means, a deficit of $D = 0.00609$ is needed to be provided by the outer voltage loop. In addition, for a change in the supply voltage in the positive direction, the duty cycle has to decrease in order to maintain the output voltage constant. Therefore, the phase difference between the input voltage and duty cycle is $-180°$.

2.7.6 Input Impedance Z_{iicl}

Using the block diagram shown in Fig. 2.43, the closed-loop input admittance is

$$Z_{iicl}(s) = \frac{v_i(s)}{i_i(s)}. \tag{2.162}$$

From Fig. 2.43,

$$i_l = i_l' + i_l'' = T_{pi}d + M_{vi}v_i \tag{2.163}$$

to give

$$d = \frac{i_l}{T_{pi}} - \frac{M_{vi}}{T_{pi}}v_i. \tag{2.164}$$

Also

$$i_l = T_{pi}(T_m T_{ci} v_{ei}) + M_{vi}v_i = T_{pi}T_m T_{ci}(-T_f R_s i_l) + M_{vi}v_i = -T_i i_l + M_{vi}v_i. \tag{2.165}$$

Rearrangement of (2.165) yields

$$i_l(1 + T_i) = M_{vi}v_i. \tag{2.166}$$

Hence

$$i_l = \frac{M_{vi}}{1 + T_i}v_i. \tag{2.167}$$

The input current is given as

$$i_i = Di_l + I_L d. \tag{2.168}$$

Substituting d from (2.164) in (2.168), we get

$$i_i = Di_l + I_L d = Di_l + I_L\left(\frac{i_l}{T_{pi}} - \frac{M_{vi}v_i}{T_{pi}}\right) \tag{2.169}$$

$$= \left(D + \frac{I_L}{T_{pi}}\right)i_l - \frac{I_L M_{vi}}{T_{pi}}v_i. \tag{2.170}$$

Substituting (2.167) in (2.169)

$$i_i = \left[\left(D + \frac{I_L}{T_{pi}}\right)\frac{M_{vi}}{1 + T_i} - \frac{I_L M_{vi}}{T_{pi}}\right]v_i. \tag{2.171}$$

Hence, the closed-loop input admittance is

$$Y_{iicl}(s) = \frac{i_i(s)}{v_i(s)} = \left(D + \frac{I_L}{T_{pi}}\right)\frac{M_{vi}}{1 + T_i} - \frac{I_L M_{vi}}{T_{pi}}. \tag{2.172}$$

The closed-loop input impedance is

$$Z_{iicl}(s) = \frac{v_i(s)}{i_i(s)} = \frac{1}{Y_{iicl}(s)}. \tag{2.173}$$

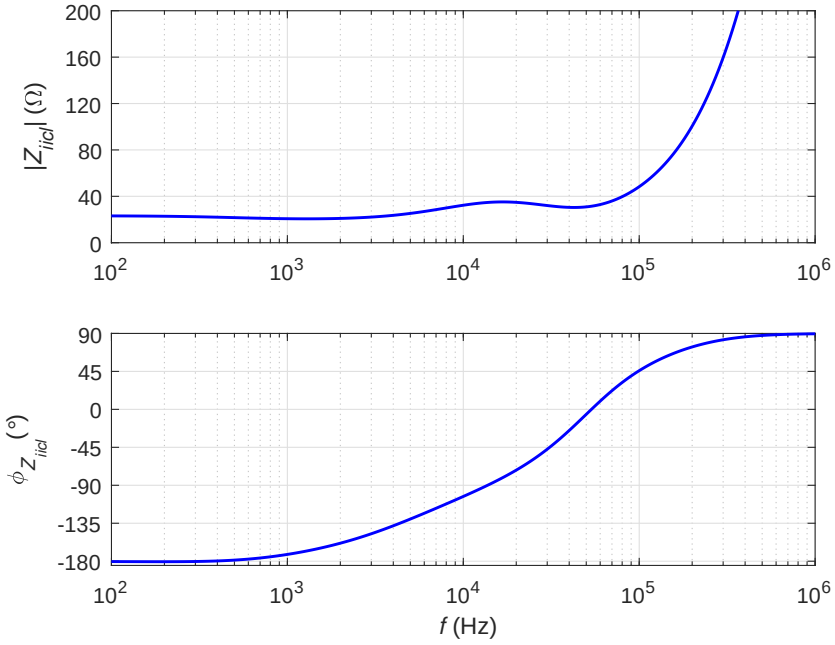

Figure 2.44: Theoretically obtained magnitude and phase plots of inner-loop input impedance Z_{iicl}.

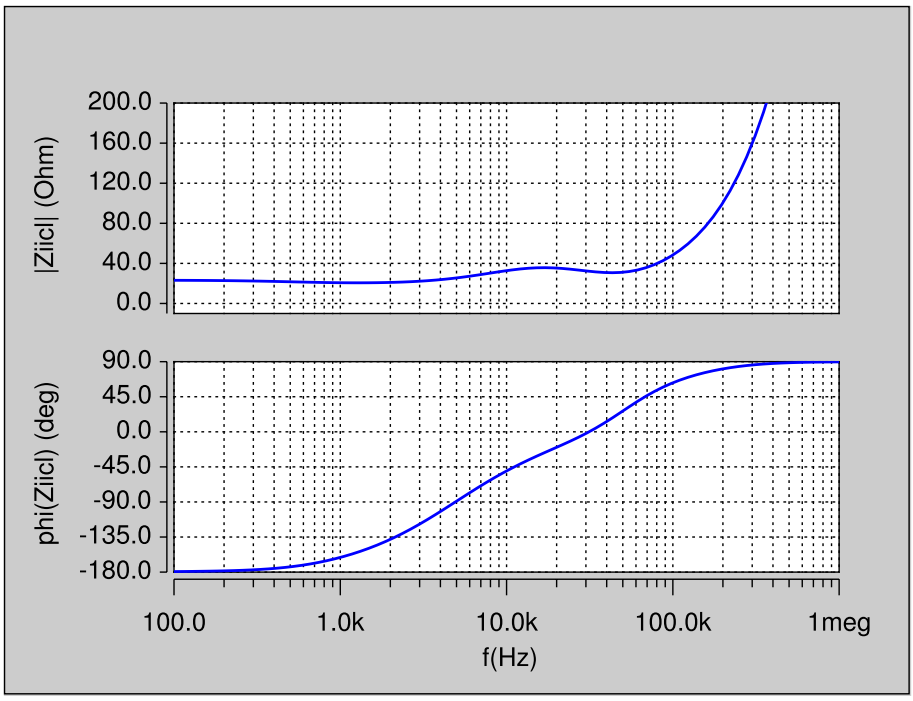

Figure 2.45: Magnitude and phase plots of inner-loop input impedance Z_{iicl} obtained by circuit simulation.

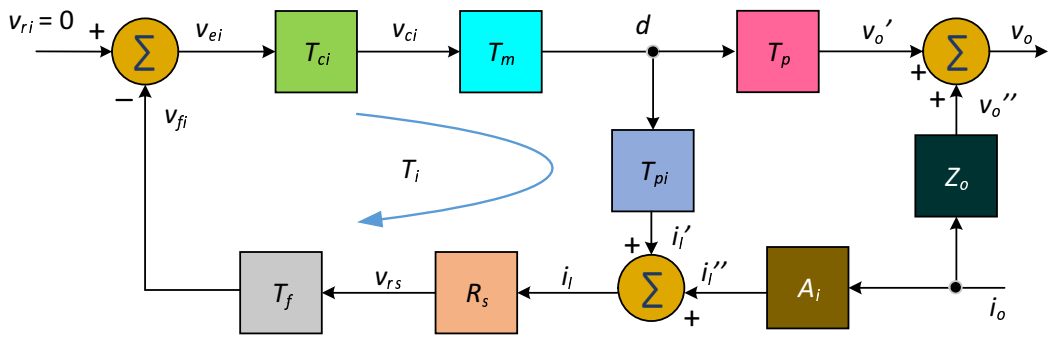

Figure 2.46: Block diagram required to derive inner-closed-loop input impedance Z_{oicl}

Fig. 2.44 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop input impedance. The theoretical results were validated by simulation. Fig. 2.45 shows the magnitude and phase plots of the inner-current loop input impedance using SABER Simulator.

2.7.7 Output Impedance Z_{oicl}

Using the block diagram shown in Fig. 2.46, the closed-loop output impedance is

$$Z_{oicl}(s) = \left.\frac{v_o(s)}{i_o(s)}\right|_{v_{ri}=v_i=0}. \tag{2.174}$$

From the block diagram

$$i_l = i_l' + i_l'' = T_{pi}d + A_i i_o \tag{2.175}$$

and

$$\frac{-d}{T_{ix}} = T_{pi}d + A_i i_o, \tag{2.176}$$

where

$$T_{ix} = \frac{T_i}{T_{pi}} = T_{ci}T_m R_s T_f. \tag{2.177}$$

Rearranging

$$-d\left(\frac{1}{T_{ix}} + T_{pi}\right) = A_i i_o. \tag{2.178}$$

Hence

$$d = -\frac{A_i T_{ix}}{1 + T_i} i_o. \tag{2.179}$$

From the block diagram in Fig. (2.46)

$$v_o = v_o' + v_o'' = T_p d + Z_o i_o. \tag{2.180}$$

Substituting d from (2.154), we get

$$v_o = T_p\left(- \frac{A_i T_{ix}}{1 + T_i} i_o \right) + Z_o i_o. = \left(Z_o - \frac{A_i T_p T_{ix}}{1 + T_i} \right) i_o. \tag{2.181}$$

The closed-loop output impedance is

$$Z_{oicl}(s) = \frac{v_o(s)}{i_o(s)} = Z_o - \frac{A_i T_p T_{ix}}{1 + T_i}. \tag{2.182}$$

Fig. 2.47 shows the theoretically obtained magnitude and phase plots of the inner-current loop output impedance. The theoretical results were validated by simulation. Fig. 2.48 shows the magnitude and phase plots of the inner-current loop output impedance using SABER Simulator. A good agreement between the theoretically predicted and SABER results can be observed for all transfer functions.

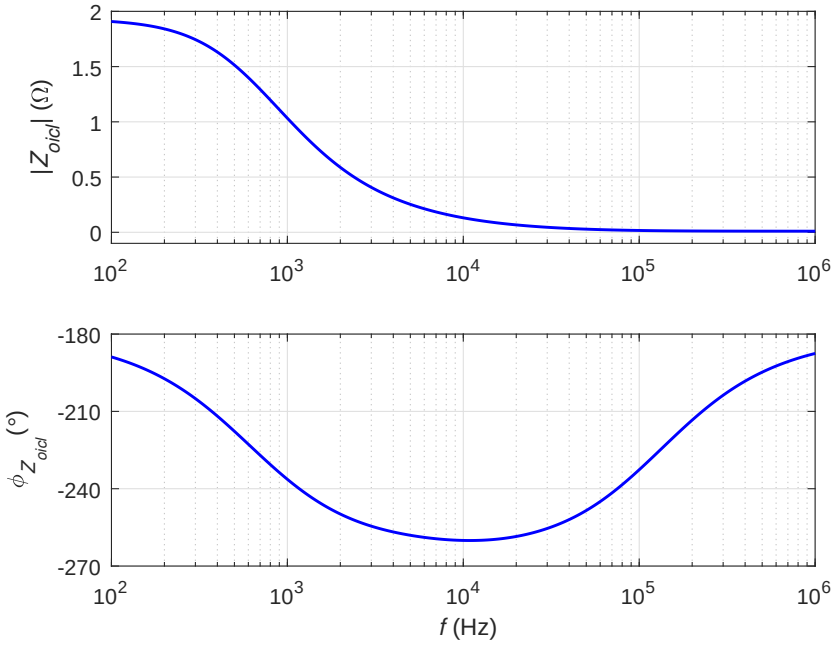

Figure 2.47: Theoretically obtained magnitude and phase plots of inner-closed loop output impedance Z_{oicl}.

2.8 Outer-Voltage Loop

The outer-voltage loop or the major loop is essential in a converter in order to act against the nonlinear disturbances in the load. With change in the load resistance, the load current increases or decreases causing the inductor current to change. However, in order to maintain the output voltage constant, it is essential to introduce the outer voltage-loop with a set reference voltage V_{RV} that regulates the output voltage. In a typical two-loop system, the reference voltage to the outer loop is a fraction of the rated output voltage. The fraction is determined by the feedback network, whose voltage gain β is determined by a network of resistors. The reference voltage must be positive. However, the output voltage is negative. Therefore, the feedback network gain β must be negative in order to have zero phase shift in the uncompensated loop gain at dc and low frequencies. The negative feedback factor can be achieved by various means, mostly depending upon the application and the type of control

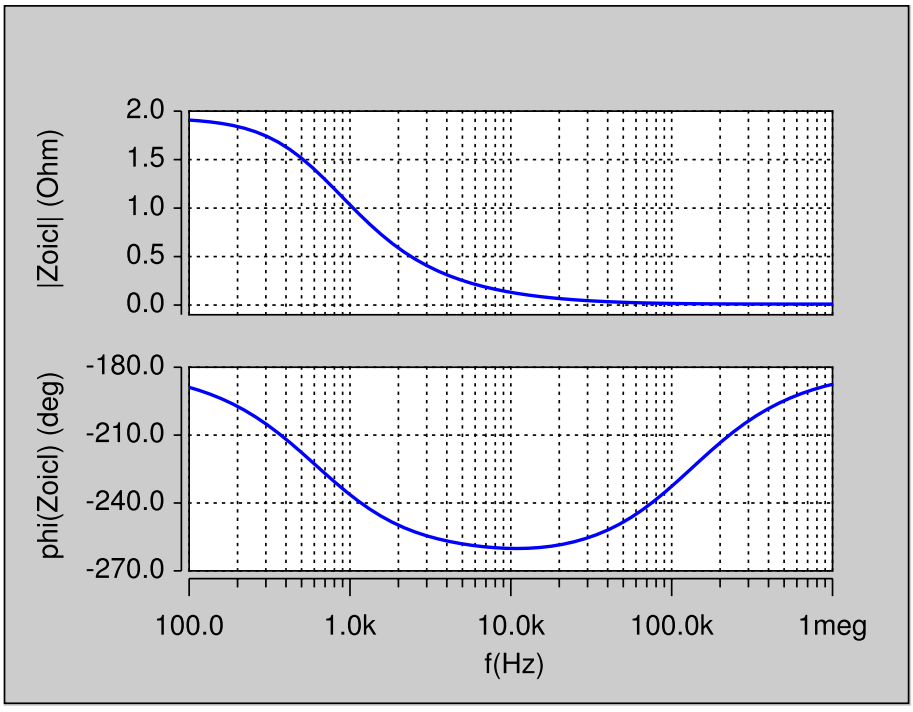

Figure 2.48: Magnitude and phase plots of inner-closed loop output impedance Z_{oicl} obtained by simulations.

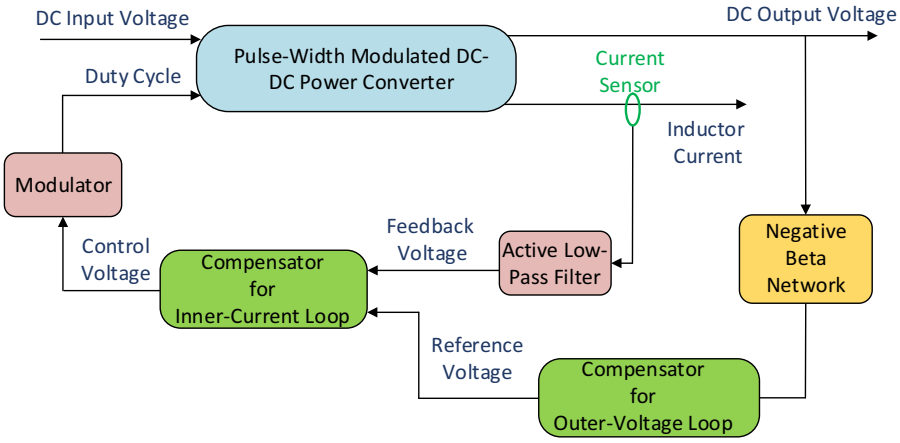

Figure 2.49: Architecture of the complete true-average current-mode controlled buck-boost converter with voltage-mode control.

(analog or digital). The block diagrams shown in the subsequent sections consist of β, whose value is negative.

Fig. 2.49 shows a complete block diagram of the true-average current-mode controlled buck-boost converter with two-loop control. Fig. 2.50 shows the circuit schematic of the buck-boost converter with true-average controlled inner-current loop and outer-voltage loop. It must be noted that the circuit schematic already includes the compensation scheme needed for the outer loop. A complete derivation of the same is provided in the subsequent sections. The feedback gain is negative in order to account for the negative output voltage. The reference voltage V_{RI} for the current loop is set by the outer loop. Typically, the bandwidth of the outer loop is slow and that of the inner-loop is fast. These aspects are discussed henceforth and validated through analytical and simulation results. Fig. 2.51 shows the SABER schematic of small-signal model of true-average current-mode controlled buck-boost converter with inner-current and outer-voltage loops. Fig. 2.52 shows SABER schematic of true-average current-mode controlled buck-boost converter with components.

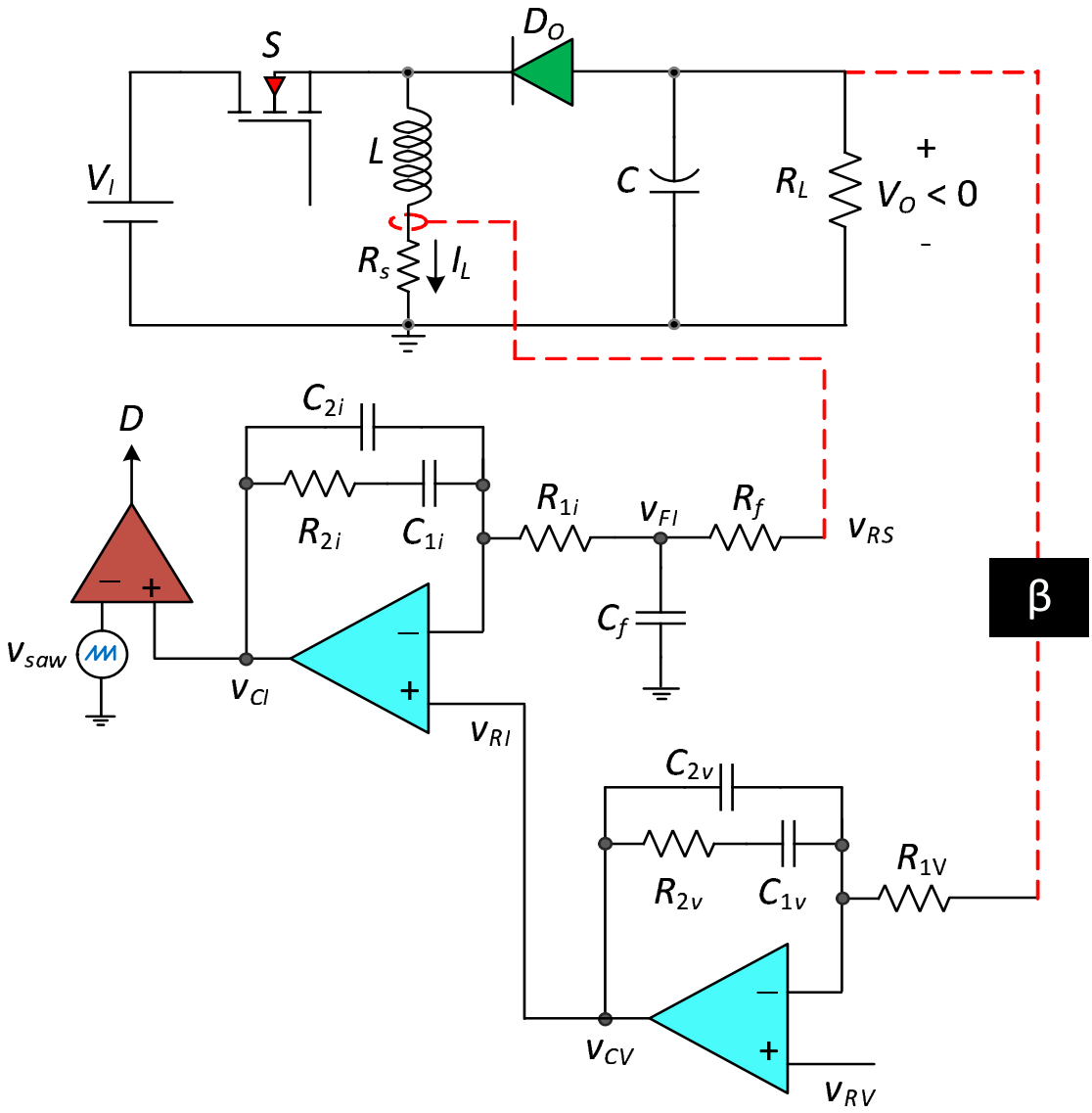

Figure 2.50: Complete circuit of true-average current-mode controlled buck-boost converter with voltage-mode control.

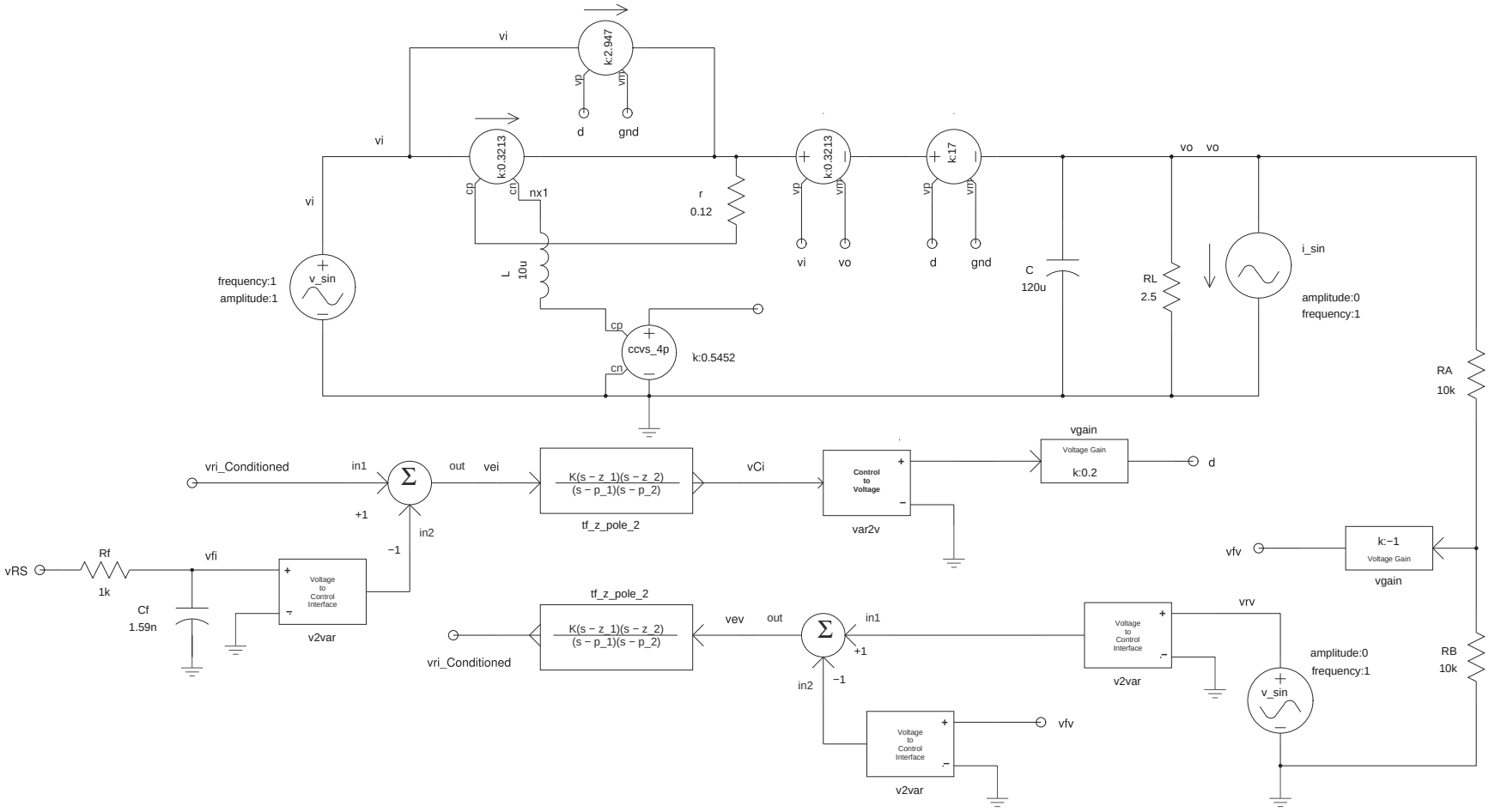

Figure 2.51: SABER schematic of small-signal model of true-average current-mode controlled buck-boost converter with inner-current and outer-voltage loops.

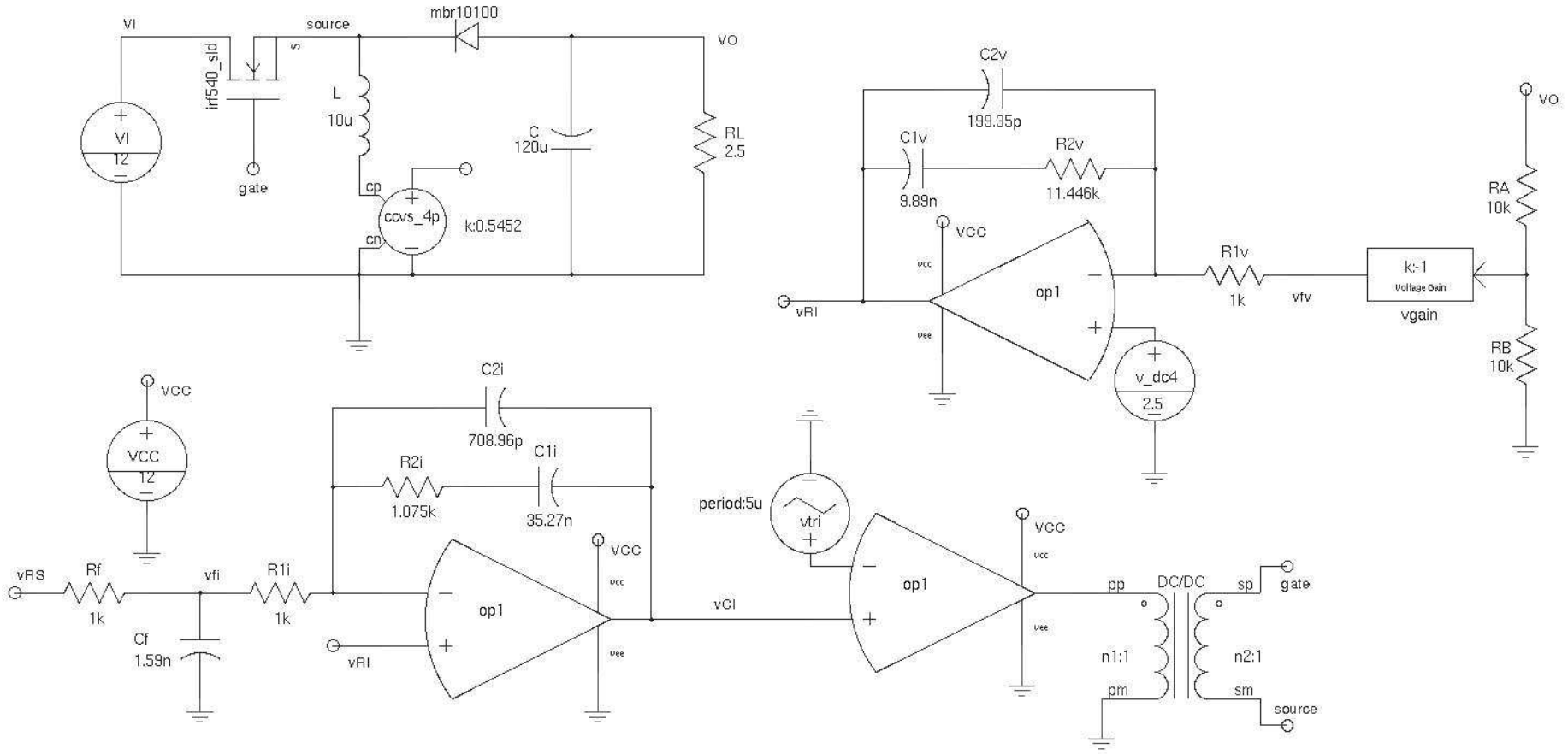

Figure 2.52: SABER schematic of true-average current-mode controlled buck-boost converter with components.

The procedure to design the outer loop is identical to that involved in designing the inner-loop. The buck-boost power stage served as the plant for the inner-current loop. However, in the case of outer-loop design, the power stage incorporated within the inner-loop serves as the plant to be controlled. Hence, the path between the current reference v_{ri} and the duty cycle d serves as the plant for the outer voltage loop. The transfer function between v_{ri} and d is a sixth order transfer function. Therefore, it is cumbersome to express the transfer functions in individual pole zero format. The complex conjugate poles in T_p, the RHP zero in T_p, the low-frequency LHP zero in T_{pi}, and the inner-current loop compensator poles are the ones, which may exist within the crossover frequency of the voltage loop gain. Therefore, attention must be paid in deciding the appropriate outer loop gain crossover frequency.

2.8.1 Uncompensated Loop Gain T_{kv}

The natural behavior of the outer-voltage-loop can be determined using the uncompensated loop gain as

$$T_{kv} = \frac{v_{fv}}{v_{ev}} = \frac{\beta v_o}{v_{ri}} = \beta T_{picl}. \tag{2.183}$$

Fig. 2.53 shows the theoretically obtained magnitude and phase plots of the outer-voltage uncompensated loop gain T_{kv}. The gain is low at dc and is nearly 1.39 dB. The crossover frequency is nearly 388 Hz. The phase margin at the crossover frequency is 150°. It is essential to provide a high gain at dc to reduce the steady-state error. The crossover frequency must be high for improved bandwidth; however, not higher than the frequency of the RHP zero present in the T_p transfer function. A significant phase boost must also be maintained at the crossover frequency in order to obtain a phase margin of 60°. Therefore, high-order control schemes such as Type-II or Type-III is much preferred for this application. The Type-II or the single-lead integral control circuit is adopted here. The design was mentioned previously in the design of the

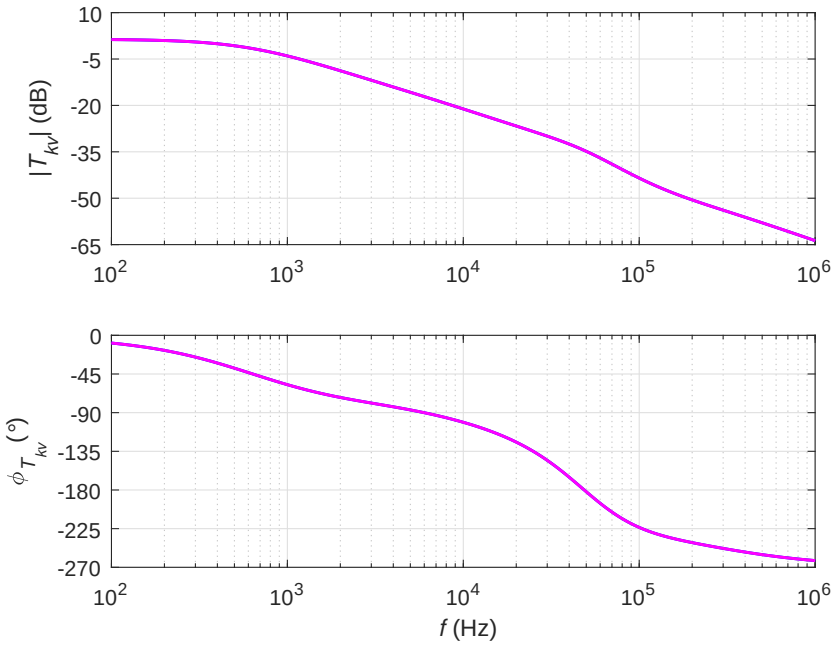

Figure 2.53: Theoretically obtained magnitude and phase plots of uncompensated loop gain T_{kv}.

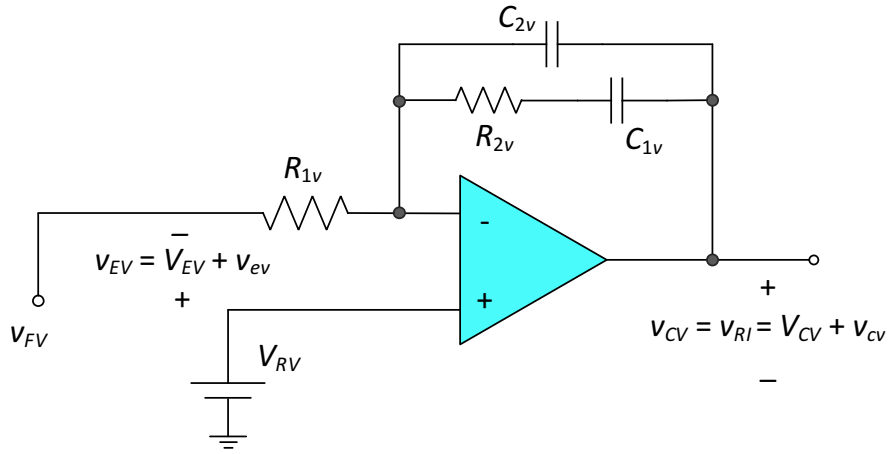

Figure 2.54: Circuit of type-II compensator used in outer-voltage loop.

inner current loop and only the voltage-loop relevant expressions are presented here. Fig. 2.54 shows the control circuit for the outer-voltage loop.

2.8.2 Transfer Function of Compensation Circuit T_{cv}

From the uncompensated loop gain transfer function T_{kv}, the crossover frequency is $f_c = 388$ Hz. A crossover frequency of $f_c = 10$ kHz is assumed in the following discussion. At the new value of f_c, the magnitude of $T_{kv}(f_c) = -21.2$ dB $= 0.871$ and the phase is $\phi_{Tkv}(f_c) = -101°$. The required phase margin is $PM = 60°$. Therefore, the phase boost required at f_c is

$$\phi_m = M - \phi_{Tk}(f_c) - 90° = 71°, \tag{2.184}$$

giving the geometric mean between the compensator corner frequencies as

$$K = \tan^{-1}\left(\frac{\phi_m}{2} + 45°\right) = 5.97. \tag{2.185}$$

Assuming $R_1 = 1$ kΩ, the value of C_2 is

$$C_2 = \frac{|T_k(f_c)|}{2\pi f_c K R_1} = 232 \text{ pF}. \tag{2.186}$$

The expression for C_1 is

$$C_1 = C_2(K^2 - 1) = 8 \text{ nF}. \tag{2.187}$$

The expression for R_2 is

$$R_2 = \frac{K}{2\pi f_c C_1} = 11.8 \text{ kΩ}. \tag{2.188}$$

The transfer function T_{ci} of the voltage loop control circuit is

$$T_{cv} = \frac{v_{cv}(s)}{v_{ev}(s)} = T_{cvo}\frac{1 + \frac{s}{\omega_{zcv}}}{s\left(1 + \frac{s}{\omega_{pcv}}\right)}, \tag{2.189}$$

where

$$T_{cvo} = \frac{1}{R_1(C_1 + C_2)}, \tag{2.190}$$

$$\omega_{zcv} = \frac{1}{R_2 C_1} = 10.5 \text{ krad/s}, \tag{2.191}$$

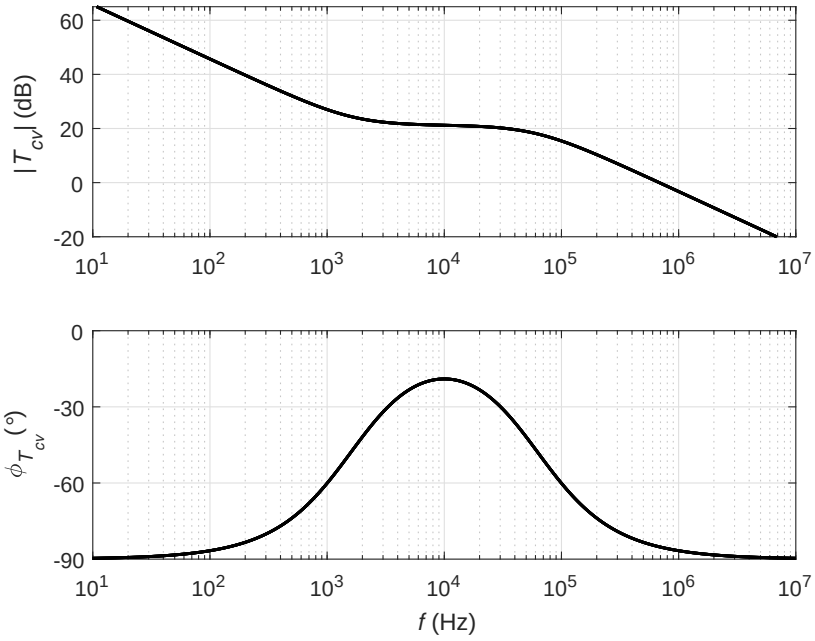

Figure 2.55: Theoretically obtained magnitude and phase plots of compensator transfer function T_{cv} for the outer-voltage loop.

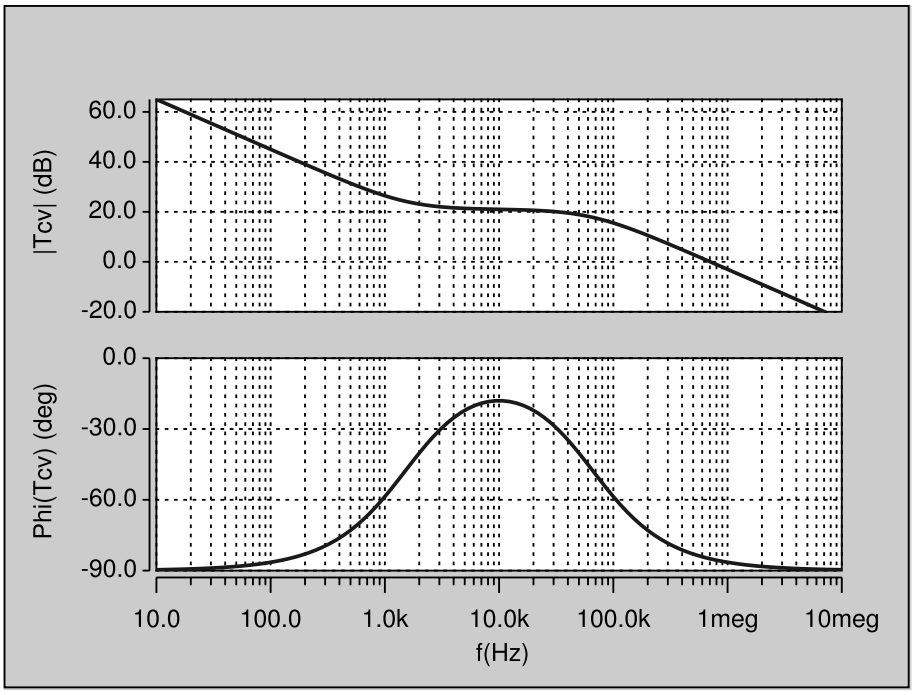

Figure 2.56: Magnitude and phase plots of the compensator transfer function T_{cv} for the outer-voltage loop obtained by circuit simulation.

and

$$\omega_{pcv} = \frac{C_1 + C_2}{R_2 C_1 C_2} = 375.5 \text{ krad/s}. \tag{2.192}$$

Fig. 2.55 shows the theoretically obtained magnitude and phase plots of the compensator transfer function used in the outer-voltage loop. The theoretical results were validated by simulation. Fig. 2.56 shows the magnitude and phase plots of the compensator transfer function used in the outer-voltage loop using SABER Simulator. The poles are located at 0 Hz and 59.75 kHz and the zero is located at 1.67 kHz. A phase boost of nearly 70° is provided at a crossover frequency of 10 kHz.

2.8.3 Compensated Loop Gain T_v

The loop gain of the compensated outer-voltage loop is

$$T_v = \frac{v_{ev}}{v_{fv}} = T_{kv} T_{cv}. \tag{2.193}$$

The order of transfer function of T_v is eight. It is cumbersome to describe factorized form of these transfer functions. However, such a system can be very easily handled by computationally efficient tool such as MATLAB.

Fig. 2.8.3 shows the theoretically obtained magnitude and phase plots of the loop gain of compensated outer-voltage loop. The theoretical results were validated by simulation. Fig. 2.58 shows the magnitude and phase plots of the loop gain of compensated outer-voltage loop using SABER Simulator. The outer voltage loop gain has a phase margin of 60°. The gain at dc is higher than 60 dB. A high gain at dc was already contributed by the high gain property of the current loop plant.

2.9 Closed-Loop Transfer Functions for Outer-Voltage Loop

The following closed-loop transfer functions are derived

- Reference voltage-to-output voltage transfer function T_{pcl} (Control).

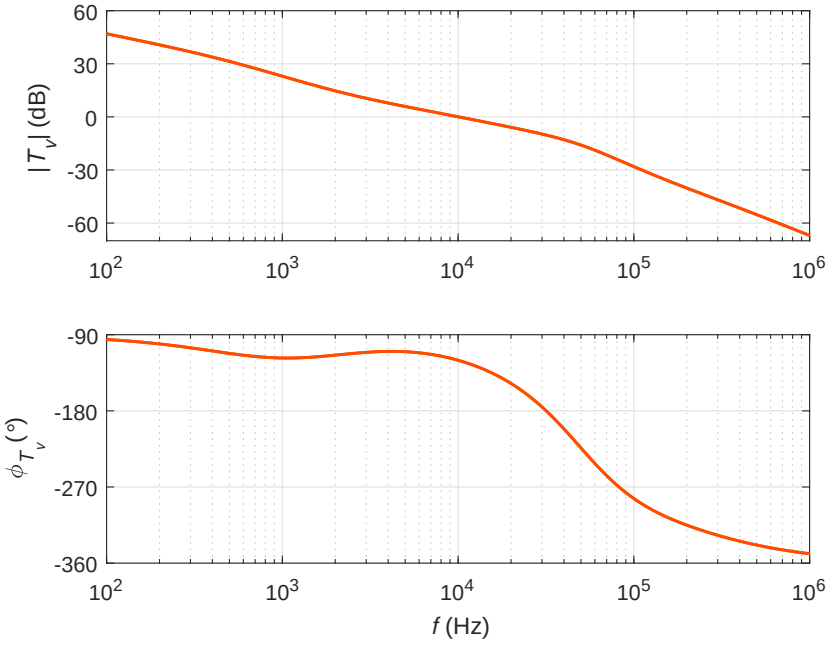

Figure 2.57: Theoretically obtained magnitude and phase plots of the loop gain T_v of the compensated outer-voltage loop.

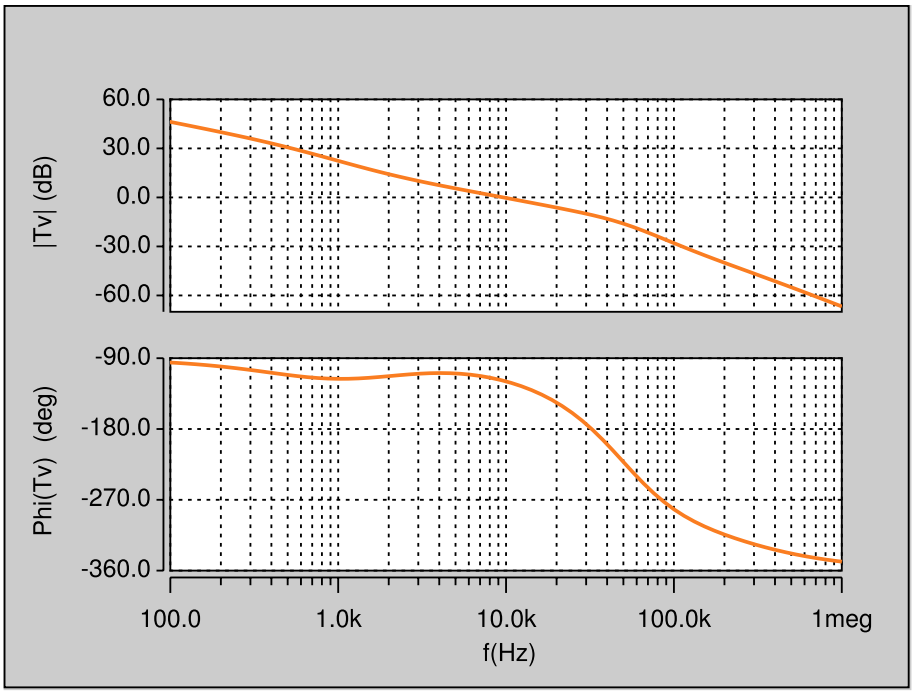

Figure 2.58: Magnitude and phase plots of the loop gain T_v of the compensated outer-voltage loop obtained by circuit simulation.

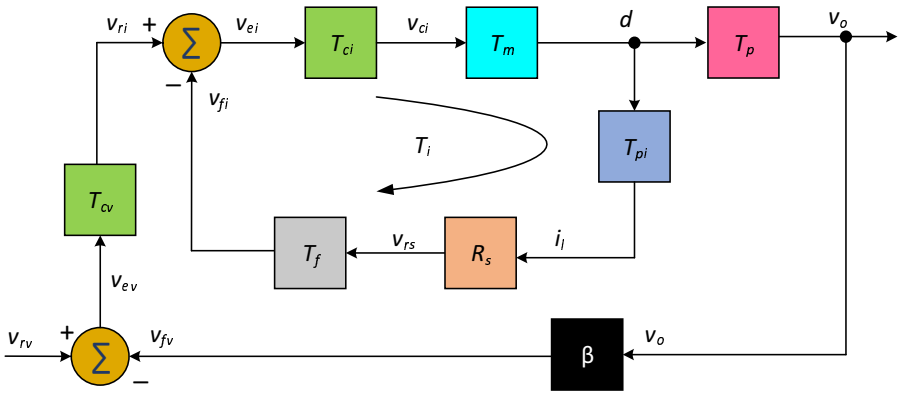

Figure 2.59: Block diagram used to derive control-to-output voltage transfer function T_{pcl}.

- Input voltage-to-output voltage transfer function M_{vcl} (Disturbance).
- Input voltage-to-duty cycle transfer function M_{dv} (Disturbance).
- Input impedance Z_{ivcl} (Disturbance).
- Output impedance Z_{ovcl} (Disturbance).

2.9.1 Reference Voltage-to-Output Voltage Transfer Function T_{pcl}

Using the block diagram shown in Fig. 2.59, the closed-loop reference voltage-to-output voltage transfer function is

$$T_{pcl}(s) = \frac{v_o(s)}{v_{rv}(s)} = \frac{T_{cv}T_{picl}}{1+T_v}. \tag{2.194}$$

Fig. 2.60 shows the theoretically obtained magnitude and phase plots of the reference voltage-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 2.61 shows the magnitude and phase plots of the reference voltage-to-output voltage transfer function using SABER Simulator.

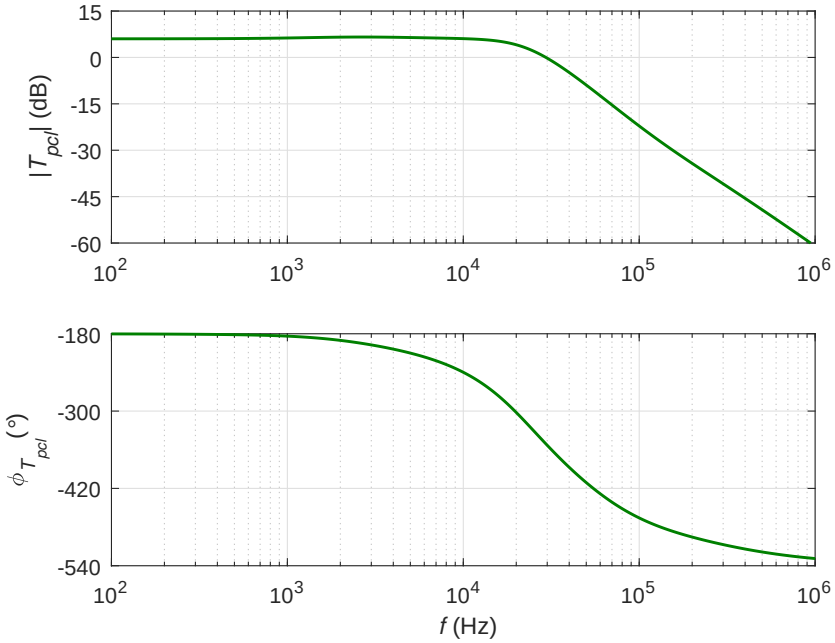

Figure 2.60: Theoretically obtained magnitude and phase plots of the reference voltage-to-output voltage transfer function T_{pcl}.

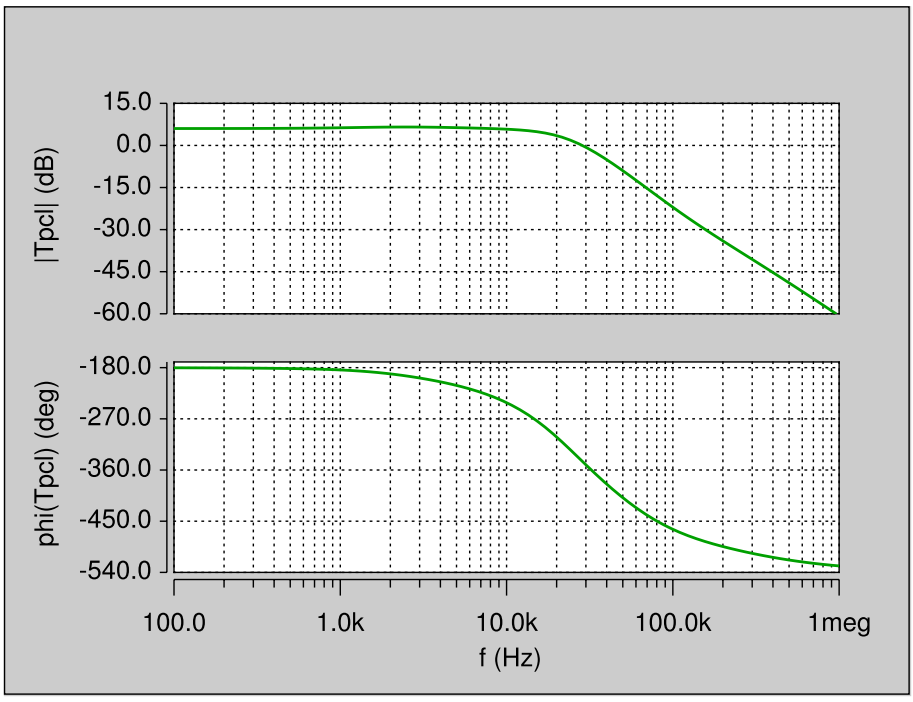

Figure 2.61: Magnitude and phase plots of the reference voltage-to-output voltage transfer function T_{pcl} obtained by circuit simulation.

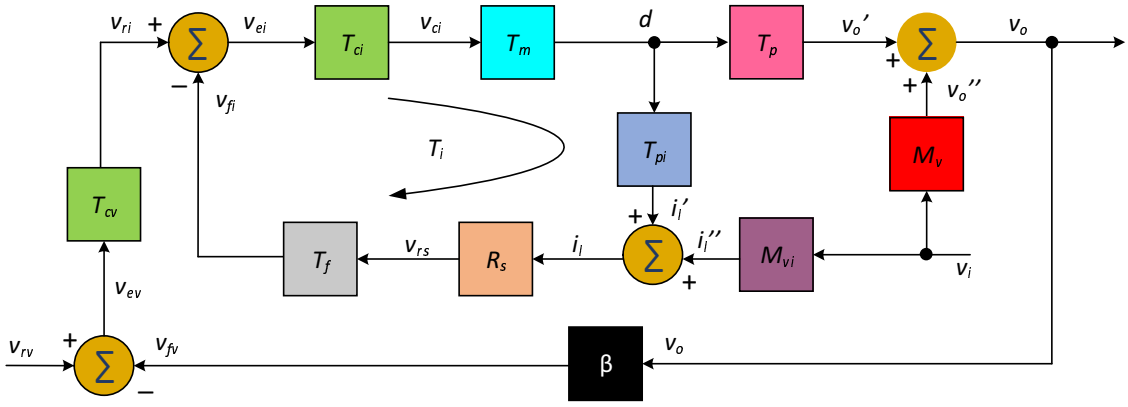

Figure 2.62: Block diagram used to derive the input voltage to duty cycle transfer function M_{dv}.

2.9.2 Input Voltage-to-Duty Cycle Transfer Function M_{dv}

Using the block diagram shown in Fig. 2.62, the closed-loop input voltage to duty cycle transfer function is

$$M_{dv}(s) = \frac{d(s)}{v_i(s)}. \tag{2.195}$$

From the block diagram

$$v_o = v_o' + v_o'' = T_p d + M_v v_i. \tag{2.196}$$

Also

$$v_{fv} = -\beta v_o \tag{2.197}$$

and

$$v_{cv} = v_{ri} = -\beta T_{cv} v_o. \tag{2.198}$$

The error voltage v_{ei} is

$$v_{ei} = v_{ri} - v_{fi} = -T_{cv}\beta v_o - R_s T_f i_l, \tag{2.199}$$

and

$$v_{ei} = \frac{d}{T_m T_{ci}}. \tag{2.200}$$

The inductor current is

$$i_l = T_{pi} d + M_{vi} v_i. \tag{2.201}$$

Substituting (2.201) and (2.200) in (2.199), yeilds

$$\frac{d}{T_m T_{ci}} = -T_{cv}\beta v_o - R_s T_f (T_{pi} d + M_{vi} v_i). \tag{2.202}$$

Rearranging

$$v_o = -\frac{d}{T_{cv}\beta}\left(\frac{1}{T_m T_{ci}} + R_s T_f T_{pi}\right) - \frac{v_i}{T_{cv}\beta}\left(R_s T_f M_{vi}\right). \tag{2.203}$$

Equating (2.196) and (2.203) and rearranging

$$v_i\left(-\frac{M_{vi} R_s T_f}{T_{cv}\beta} - M_v\right) = d\left(T_p + \frac{1}{T_m T_{ci} T_{cv}\beta} + \frac{R_s T_f T_{pi}}{T_{cv}\beta}\right). \tag{2.204}$$

Simplifying further

$$-\frac{v_i}{T_{cv}\beta}\left(M_{vi} R_s T_f + M_v T_{cv}\beta\right) = \frac{d}{T_{cv}\beta}\left(T_p T_{cv}\beta + \frac{1 + R_s T_f T_{pi} T_m T_{ci}}{T_m T_{ci}}\right) \tag{2.205}$$

and

$$-v_i\left(M_{vi} R_s T_f + M_v T_{cv}\beta\right) = d\left(T_p T_{cv}\beta + \frac{1 + R_s T_f T_{pi} T_m T_{ci}}{T_m T_{ci}}\right). \tag{2.206}$$

Hence

$$M_{dv}(s) = \frac{d(s)}{v_i(s)} = -\frac{M_{vi} R_s T_f + \beta M_v T_{cv}}{\beta T_p T_{cv} + \dfrac{1 + T_i}{T_m T_{ci}}} = -\frac{T_{ci} T_m (M_{vi} R_s T_f + \beta M_v T_{cv})}{\beta T_p T_{cv} T_{ci} T_m + 1 + T_i}. \tag{2.207}$$

Fig. 2.63 shows the theoretically obtained magnitude and phase plots of the input voltage-to-duty cycle transfer function. The theoretical results were validated by simulation. Fig. 2.64 shows the magnitude and phase plots of the input voltage-to-duty cycle transfer function using SABER Simulator. This analysis is being reported for the first time in form of transfer functions. From the Bode plot, the magnitude of the transfer function at dc is nearly $M_{dv0} = 0.017$, i.e., for a step change in input voltage by 1 V, the duty cycle changes by nearly 0.017 units in order to correct the disturbance. With only the inner-loop control, the change in duty cycle was merely

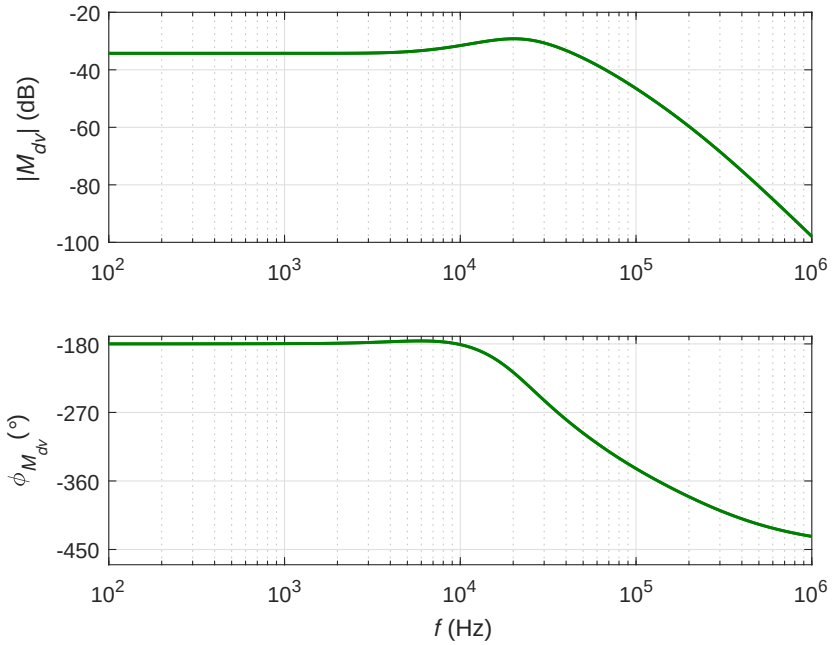

Figure 2.63: Theoretically obtained magnitude and phase plots of the input voltage-to-duty cycle transfer function M_{dv}.

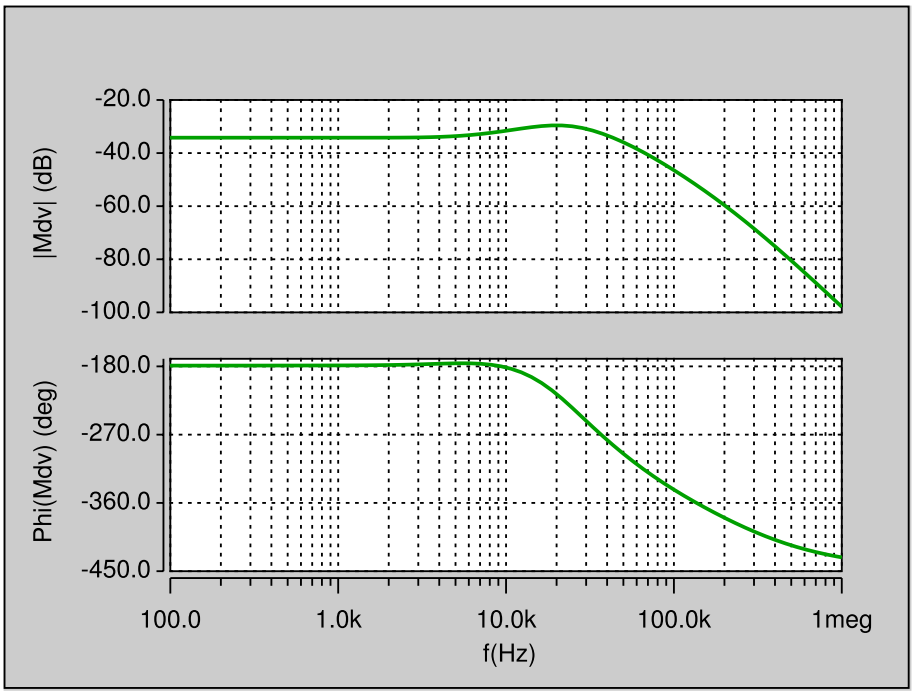

Figure 2.64: Magnitude and phase plots of the loop gain of the the input voltage-to-duty cycle transfer function M_{dv} obtained by circuit simulation.

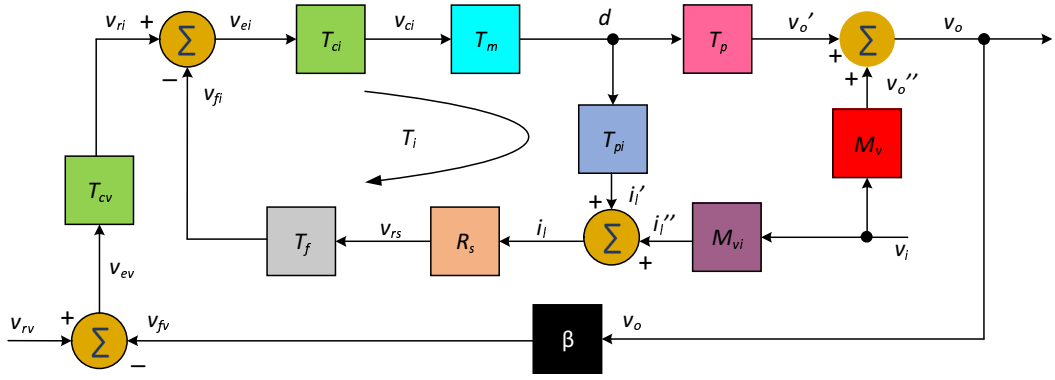

Figure 2.65: Block diagram used to derive the input voltage-to-output voltage transfer function M_{vcl}.

$M_{di0} = 0.012$ units. Consider a case, where the steady-state input voltage of the designed buck-boost converter changes from 12 V to 14 V, then the corresponding change in the duty cycle needed to maintain the output voltage V_O constant is $\Delta D = 0.0309$. However, the current loop is able to provide only $\Delta D = M_{di0} \times \Delta V_I = 0.017 \times 2 = 0.034$ units. This means that the outer loop is able to completely compensate for any change in the input voltage and achieve tightly controlled output voltage maintained at $V_O = 5$ V. In addition, for a change in the supply voltage in the positive direction, the duty cycle has to decrease in order to maintain the output voltage constant. Therefore, the phase difference between the input voltage and duty cycle is $-180°$.

2.9.3 Input Voltage-to-Output Voltage Transfer Function M_{vcl}

Using the block diagram shown in Fig. 2.65, the closed-loop input voltage to output voltage transfer function with outer-voltage-loop is

$$M_{vcl}(s) = \frac{v_o(s)}{v_i(s)}. \tag{2.208}$$

From (2.195)

$$d = M_{dv} v_i. \tag{2.209}$$

Substituting (2.209) in (2.196)

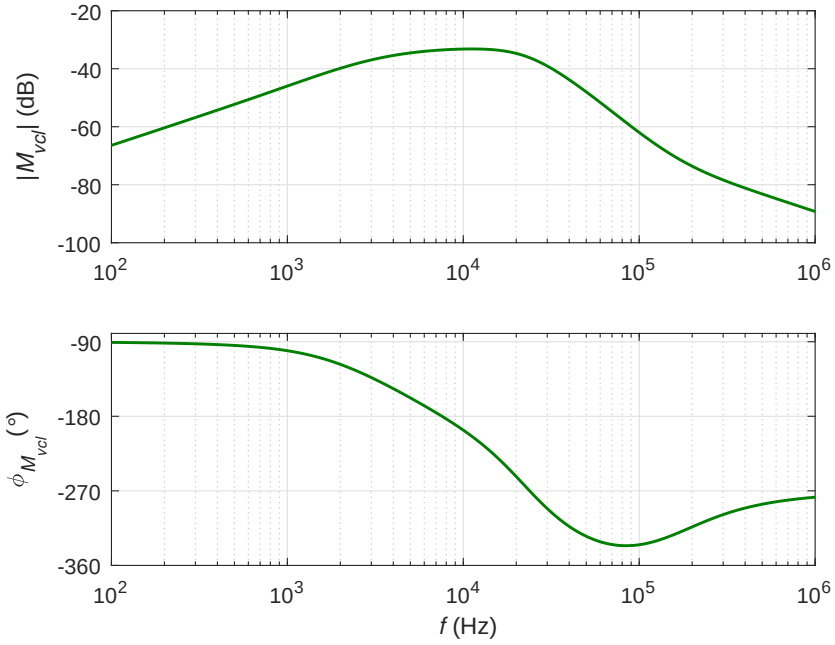

Figure 2.66: Theoretically obtained magnitude and phase plots of the input voltage-to-output voltage transfer function M_{vcl}.

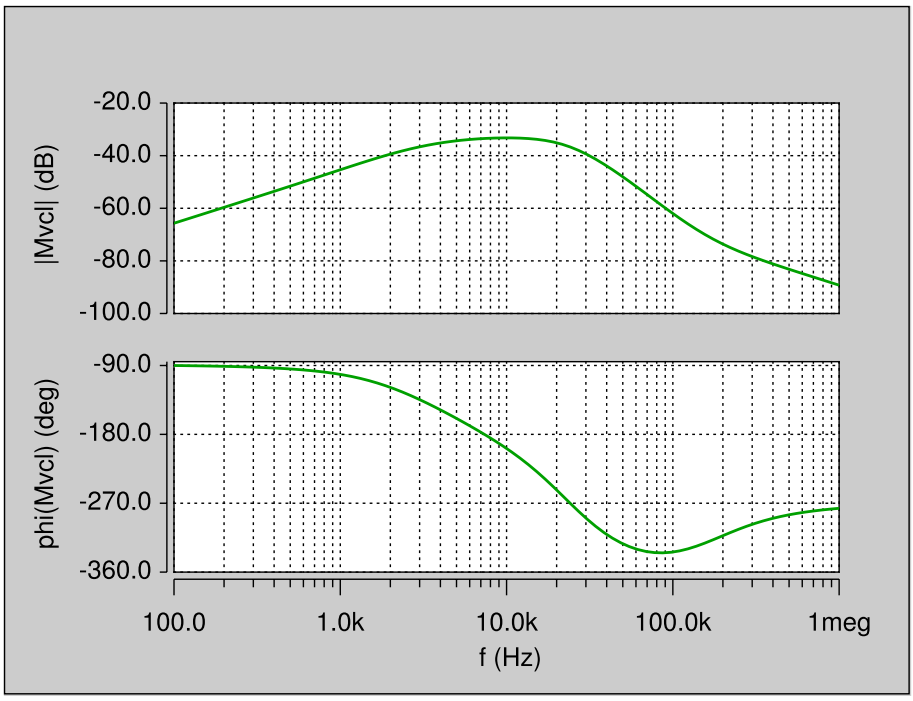

Figure 2.67: Magnitude and phase plots of the loop gain the input voltage-to-output voltage transfer function M_{vcl} obtained by circuit simulation.

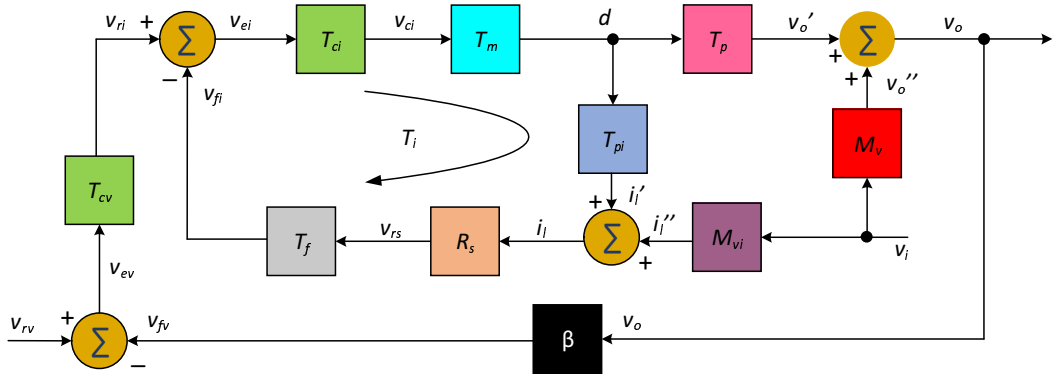

Figure 2.68: Block diagram used to derive the closed outer-voltage loop input impedance Z_{ivcl}.

$$v_o = v_o' + v_o'' = T_p d + M_v v_i = T_p M_{dv} v_i + M_v v_i. \tag{2.210}$$

Rearrangement of (2.210) yeilds

$$M_{vcl}(s) = \frac{v_o(s)}{v_i(s)} = T_p M_{dv} + M_v. \tag{2.211}$$

Fig. 2.66 shows the theoretically obtained magnitude and phase plots of the input voltage-to-output voltage transfer function M_{vcl}. The theoretical results were validated by simulation. Fig. 2.67 shows the magnitude and phase plots of the input voltage-to-output voltage transfer function M_{vcl} using SABER Simulator. By comparing the results of M_{vicl} and M_{vcl}, it can be observed that the outer-voltage loop provides a stronger attenuation to disturbances in the input voltage, than that offered by the inner current loop alone. The attenuation is stronger at low dc and low frequencies. However, at high frequencies, approximately beyond f_c, the transfer function takes the form of M_{vicl}, where the negative feedback is almost ineffective.

2.9.4 Input Impedance Z_{ivcl}

Using the block diagram shown in Fig. 2.68, the closed-loop input impedance with outer-voltage-loop is

$$Z_{ivcl}(s) = \frac{v_i(s)}{i_i(s)}. \tag{2.212}$$

From the Fig. 2.68,

$$v_o = v_o' + v_o'' = T_p d + M_v v_i \tag{2.213}$$

and

$$i_l = i_l' + i_l'' = T_{pi} d + M_{vi} v_i. \tag{2.214}$$

Also

$$v_{fv} = \beta v_o, \tag{2.215}$$

$$v_{ev} = v_{rv} - v_{fv} = 0 - \beta v_o = -\beta v_o, \tag{2.216}$$

and

$$v_{cv} = v_{ri} = T_{cv} v_{ev} = -\beta T_{cv} v_o. \tag{2.217}$$

The error voltage v_{ei} is

$$v_{ei} = \frac{d}{T_{ci} T_m}. \tag{2.218}$$

The feedback voltage v_{fi} is

$$v_{fi} = T_f R_s i_l. \tag{2.219}$$

The reference voltage to inner-current loop is

$$v_{ri} = v_{ei} + v_{fi}. \tag{2.220}$$

Substituting (2.217), (2.218), and (2.219) in (2.220)

$$-\beta T_{cv} v_o = \frac{d}{T_{ci} T_m} + T_f R_s i_l. \tag{2.221}$$

Rearranging

$$v_o = -\frac{d}{\beta T_{cv} T_{ci} T_m} - \frac{T_f R_s i_l}{\beta T_{cv}}. \tag{2.222}$$

Substituting (2.213) in (2.222)

$$T_p d + M_v v_i = -\frac{d}{\beta T_{cv} T_{ci} T_m} - \frac{T_f R_s i_l}{\beta T_{cv}}. \tag{2.223}$$

Rearranging

$$d\left(T_p + \frac{1}{\beta T_{cv} T_{ci} T_m}\right) = -\frac{T_f R_s i_l}{\beta T_{cv}} - M_v v_i. \tag{2.224}$$

Substituting (2.214) in (2.224)

$$d\left(T_p + \frac{1}{\beta T_{cv} T_{ci} T_m}\right) = -\frac{T_f R_s (T_{pi} d + M_{vi} v_i)}{\beta T_{cv}} - M_v v_i. \tag{2.225}$$

$$d\left(T_p + \frac{1}{\beta T_{cv} T_{ci} T_m} + \frac{T_f R_s T_{pi}}{\beta T_{cv}}\right) = \left(-\frac{T_f R_s M_{vi}}{\beta T_{cv}} - M_v\right) v_i. \tag{2.226}$$

$$d\left(\frac{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m}{\beta T_{ci} T_m T_{cv}}\right) = \left(\frac{-T_f R_s M_{vi} - \beta T_{cv} M_v}{\beta T_{cv}}\right) v_i. \tag{2.227}$$

$$d = -\frac{T_{ci} T_m (T_f R_s M_{vi} + \beta M_v T_{cv})}{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m} v_i \tag{2.228}$$

The input current i_i is

$$i_i = I_L d + D i_l = I_L d + D(T_{pi} d + M_{vi} v_i) = (I_L + D T_{pi}) d + D M_{vi} v_i. \tag{2.229}$$

Substituting (2.228) in (2.229)

$$i_i = (I_L + D T_{pi}) \left[-\frac{T_{ci} T_m (T_f R_s M_{vi} + \beta M_v T_{cv})}{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m} v_i \right] + D M_{vi} v_i. \tag{2.230}$$

$$i_i = \left[-(I_L + D T_{pi}) \frac{T_{ci} T_m (T_f R_s M_{vi} + \beta M_v T_{cv})}{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m} + D M_{vi} \right] v_i. \tag{2.231}$$

Hence, the closed-loop input admittance for outer-voltage loop is

$$Y_{ivcl}(s) = \frac{i_i(s)}{v_i(s)} = -(I_L + D T_{pi}) \frac{T_{ci} T_m (T_f R_s M_{vi} + \beta M_v T_{cv})}{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m} + D M_{vi}. \tag{2.232}$$

The closed-loop input impedance for outer-voltage loop is

$$Z_{ivcl}(s) = \frac{v_i(s)}{i_i(s)} = \frac{1}{Y_{ivcl}(s)}. \tag{2.233}$$

Fig. 2.69 shows the theoretically obtained magnitude and phase plots of the closed-loop input impedance Z_{ivcl}. The theoretical results were validated by simulation. Fig. 2.70 shows the magnitude and phase plots of the closed-loop input impedance Z_{ivcl} using SABER Simulator.

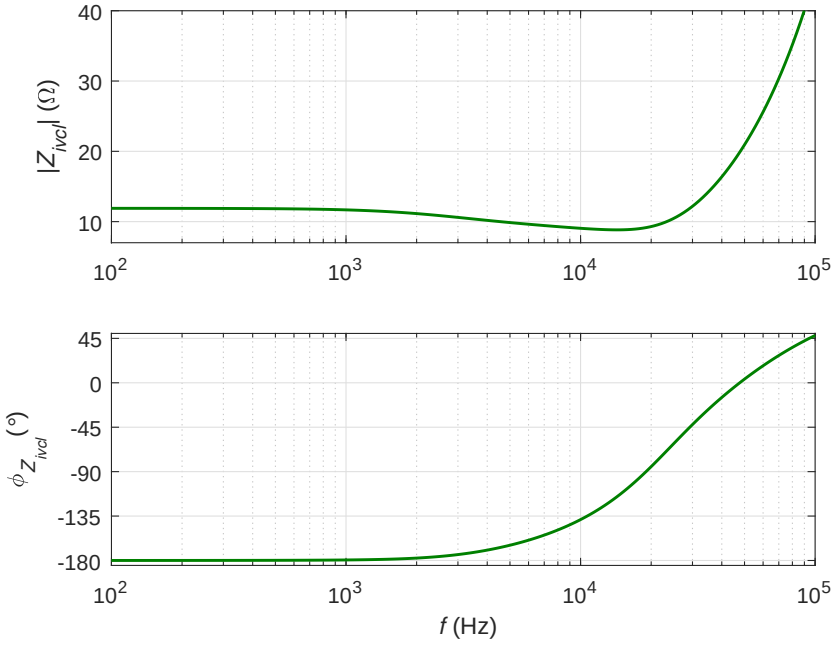

Figure 2.69: Theoretically obtained magnitude and phase plots of the closed outer-voltage loop input impedance Z_{ivcl}.

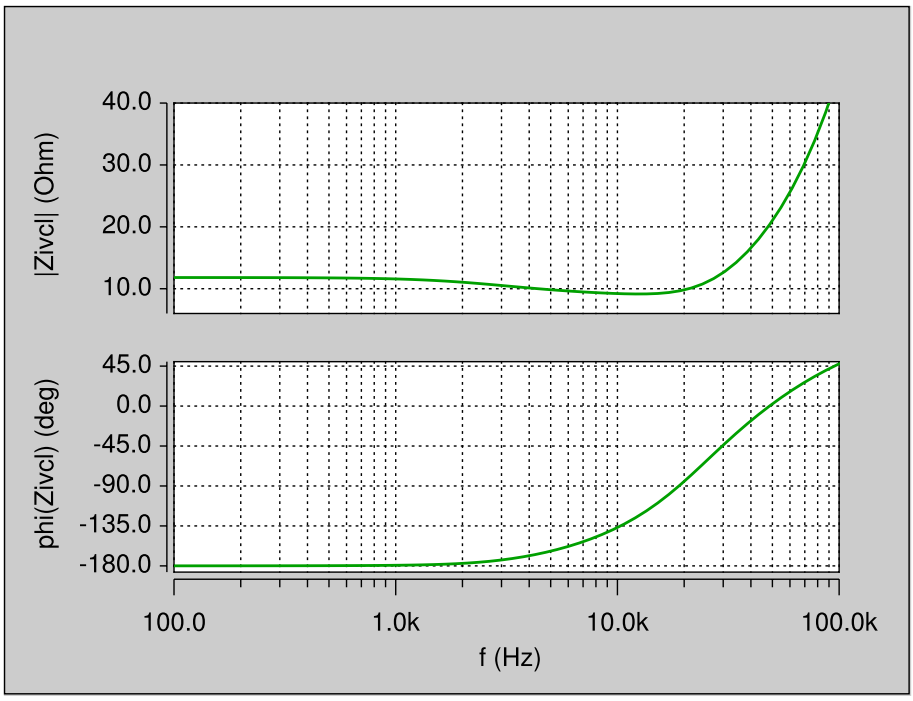

Figure 2.70: Magnitude and phase plots of the closed outer-voltage loop input impedance Z_{ivcl} obtained by circuit simulation.

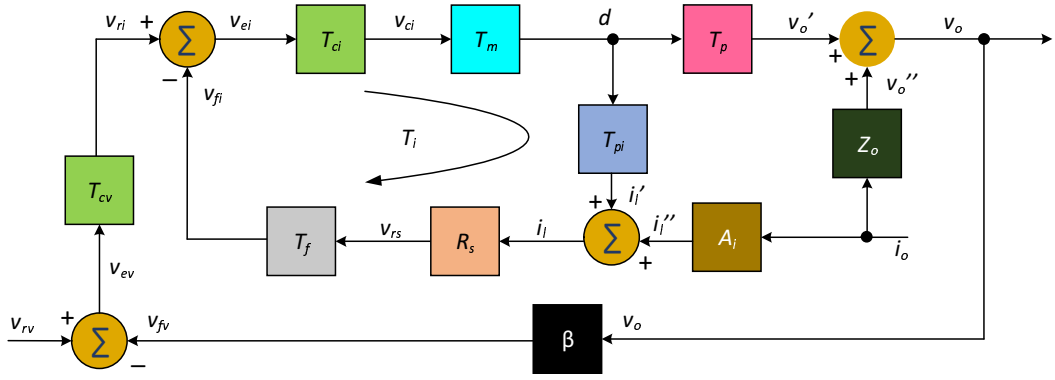

Figure 2.71: Block diagram used to derive the closed outer-voltage loop output impedance Z_{ovcl}.

2.9.5 Output Impedance Z_{ovcl}

Using the block diagram shown in Fig. 2.71, the closed-loop output impedance with outer-voltage-loop is

$$Z_{ovcl}(s) = \frac{v_o(s)}{i_o(s)}. \tag{2.234}$$

From the Fig. 2.71,

$$v_o = v_o' + v_o'' = T_p d + Z_o i_o \tag{2.235}$$

and

$$i_l = i_l' + i_l'' = A_i i_o + T_{pi} d. \tag{2.236}$$

Also

$$v_{fv} = \beta v_o \tag{2.237}$$

and

$$v_{cv} = v_{ri} = -\beta T_{cv} v_o. \tag{2.238}$$

The error voltage v_{ei} is

$$v_{ei} = v_{ri} - v_{fi} = -T_{cv}\beta v_o - R_s T_f i_l \tag{2.239}$$

and

$$v_{ei} = \frac{d}{T_m T_{ci}}. \tag{2.240}$$

Substituting (2.236) and (2.240) in (2.239), yields

$$\frac{d}{T_m T_{ci}} = -T_{cv}\beta v_o - R_s T_f (A_i i_o + T_{pi} d). \tag{2.241}$$

Rearranging (2.241)

$$d = -\frac{(T_{cv}\beta v_o + R_s T_f A_i i_o) T_{ci} T_m}{1 + T_i}. \tag{2.242}$$

Substituting (2.242) in (2.235), yields

$$v_o = T_p \left[-\frac{(T_{cv}\beta v_o + R_s T_f A_i i_o) T_{ci} T_m}{1 + T_i} \right] + Z_o i_o. \tag{2.243}$$

Rearranging

$$v_o \left(1 + \frac{\beta T_p T_{cv} T_{ci} T_m}{1 + T_i} \right) = i_o \left(Z_o - \frac{T_p R_s T_f A_i T_{ci} T_m}{1 + T_i} \right). \tag{2.244}$$

Hence, the closed-loop output impedance for outer-voltage loop is

$$Z_{ovcl}(s) = \frac{v_o(s)}{i_o(s)} = \frac{Z_o(1 + T_i) - A_i T_p T_{ix}}{1 + T_i + T_p T_{cv} \beta T_{ci} T_m}. \tag{2.245}$$

Fig. 2.72 shows the theoretically obtained magnitude and phase plots of the closed-loop output impedance Z_{ovcl}. The theoretical results were validated by simulation. Fig. 2.73 shows the magnitude and phase plots of the closed-loop output impedance Z_{ovcl} using SABER Simulator.

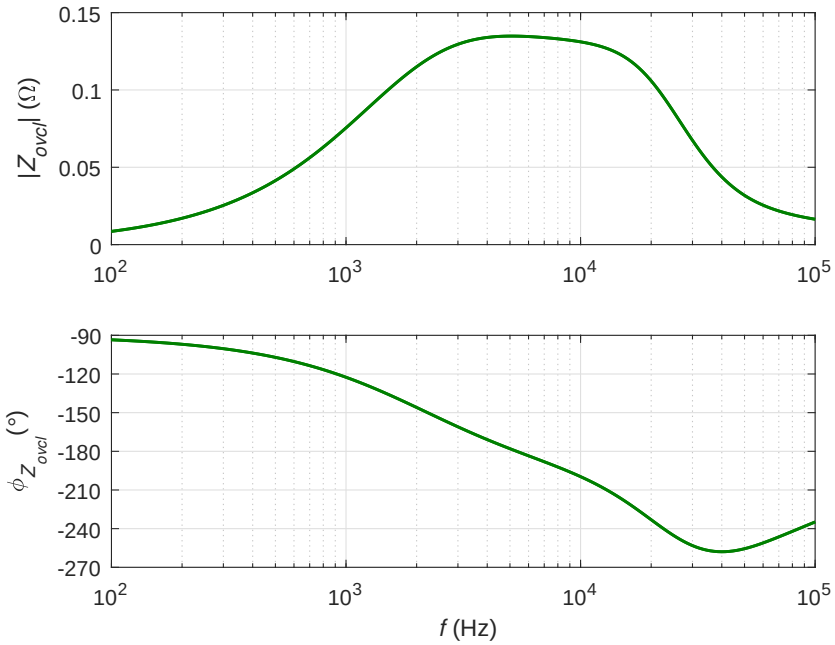

Figure 2.72: Theoretically obtained magnitude and phase plots of the closed outer-voltage loop output impedance Z_{ovcl}.

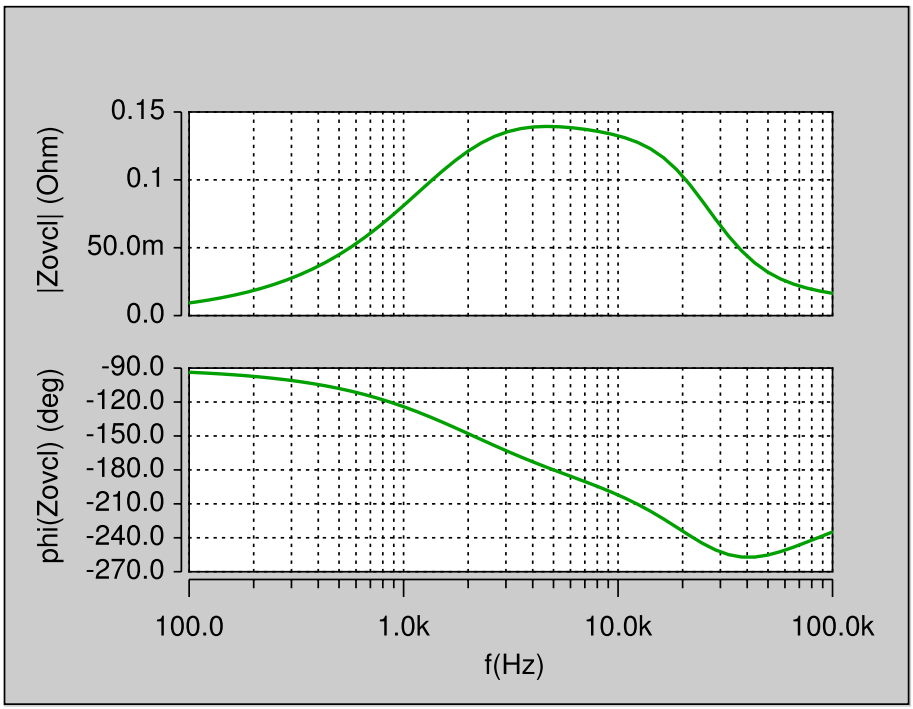

Figure 2.73: Magnitude and phase plots of the closed outer-voltage loop output impedance Z_{ovcl} obtained by circuit simulation.

3 Results: Buck-Boost DC-DC Converter

The key results of the small-signal analysis, step responses of open-loop, and closed-loop transfer functions are discussed in this section. The pole-zero plots are also presented to illustrate the relocation of the power stage poles and zeros with the introduction of inner-current and outer-voltage loops.

3.1 Open-Loop Characteristics

Fig. 3.1 compares the magnitude and phase plots of the duty cycle-to-inductor current transfer function T_{pi} and duty cycle-to-output voltage transfer function T_p. The open-loop bandwidth of T_{pi} is approximately 22 kHz, whereas the bandwidth of T_p is 5 kHz. As a result, the current loop is inherently faster than the voltage loop. Moreover, the T_{pi} transfer function produces a positive phase at frequencies around f_o. Therefore, the current-loop does not have to provide a large phase boost to achieve the desired phase margin, resulting in a simpler control schemes.

Fig. 3.3 shows the Bode magnitude and phase plots of the duty cycle-to-inductor current transfer function of the buck-boost power stage at selected values of load resistance R_L. The nominal load resistance is $R_L = 2.5\ \Omega$. The plot shows the characteristics of the T_{pi} transfer function for converter operation from full-load to light-load conditions. The plot can be described in conjunction with Fig. 3.4. Fig. 3.4 shows the variation in the damping factor with change in load resistance. The poles p_1, p_2 of T_{pi} are complex conjugate. As the load resistance R_L decreases, the damping factor ξ increases towards unity and the poles of T_{pi} move towards the real axis on the s-plane. At $R_L = 0.17\ \Omega$, the damping factor is unity and the poles of the transfer function are real and lie only on the left-half of the s-plane. With further reduction in the load resistance, the pole p_1 moves towards the origin and the pole p_2 moves towards infinity in the left-half plane. At $R_L = 50\ m\Omega$ as shown in the

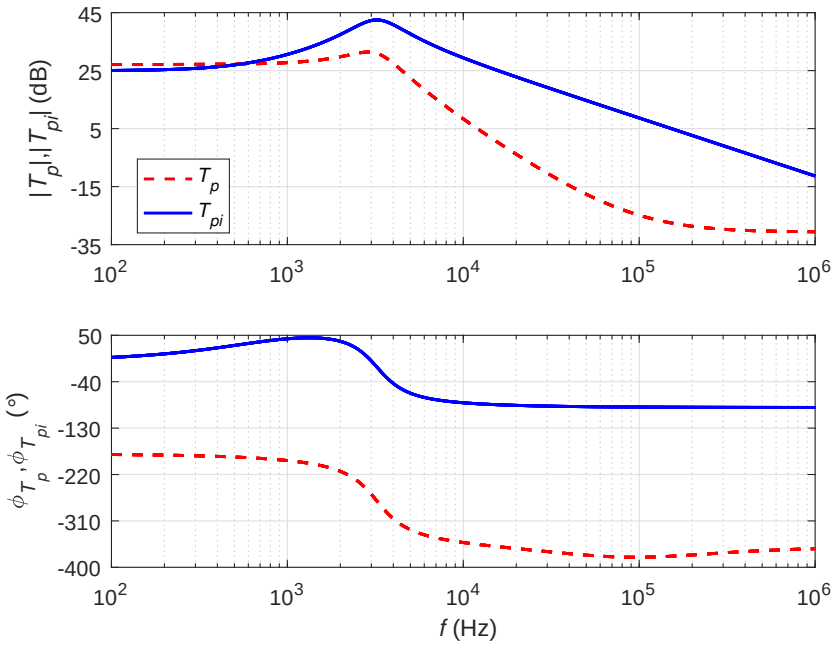

Figure 3.1: Magnitude and phase plots of the duty cycle-to-inductor current transfer function T_{pi} and duty cycle-to-output voltage transfer function T_p.

plot, the damping factor is $\xi = 1.85$, the pole p_2 approaches the zero frequency f_z and causes a pole-zero cancellation. As a result, the transfer function T_{pi} becomes first-order with a dominant pole located at

$$\omega_{p1} = -p_1 = \frac{r}{L}. \tag{3.1}$$

Therefore, the dc-dc converter produces a first-order response at high output power and the power stage transfer functions exhibit highly stable characteristics.

Fig. 3.11 shows the variation in the location of the zero z_p as a function of the duty cycle obtained using (2.35). At low duty ratios, the zero is located in the right-half of the s-plane. With increase in the duty cycle, the RHP-zero moves towards the origin. At $R_L(1-D)^2 = r$, the RHP zero is at the origin. This corresponds to a critical duty cycle determined by

$$D_{cr} = 1 - \sqrt{\frac{r}{R_L}}. \tag{3.2}$$

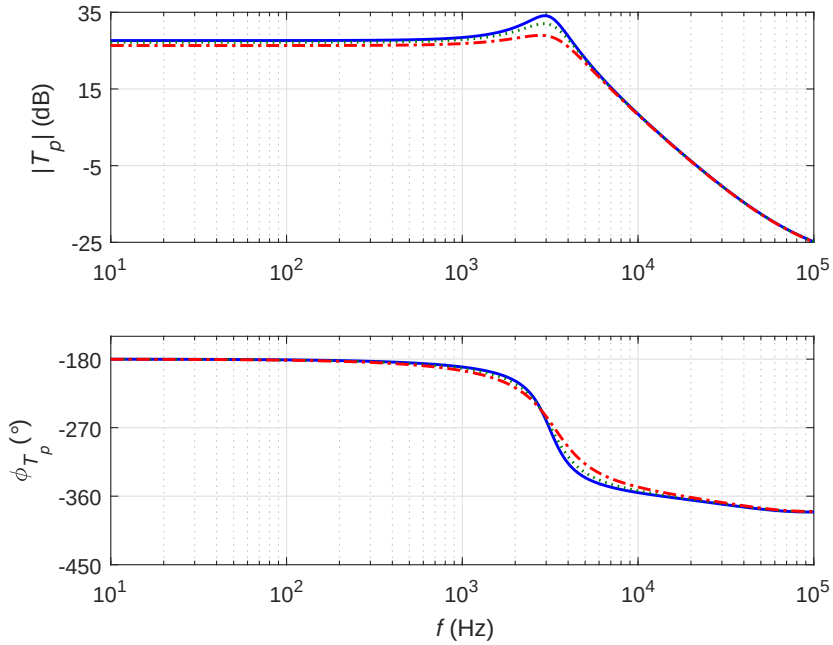

Figure 3.2: Magnitude and phase plots of the duty cycle-to-output voltage transfer function T_p at selected values of load resistance for the buck-boost dc-dc converter.

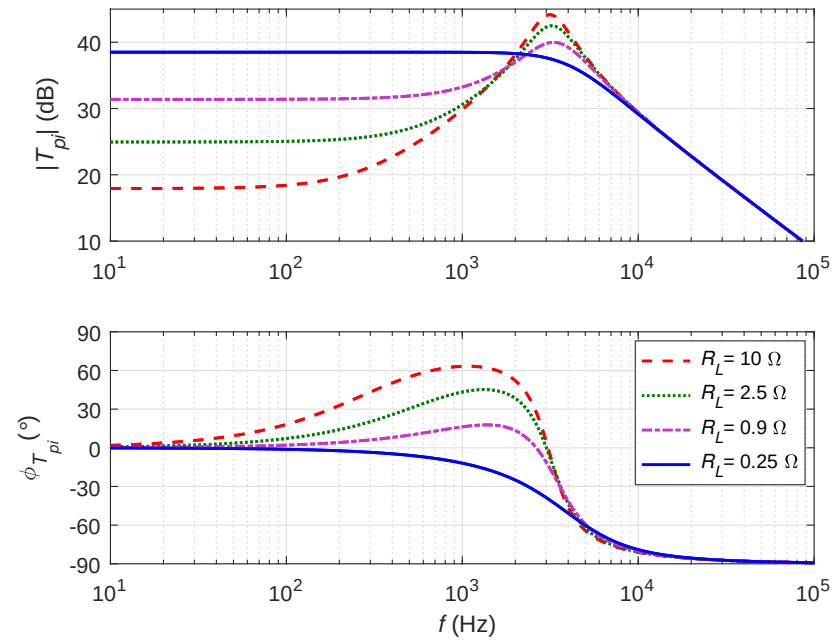

Figure 3.3: Magnitude and phase plots of the duty cycle-to-inductor current transfer function T_{pi} at selected values of load resistance for the buck-boost dc-dc converter.

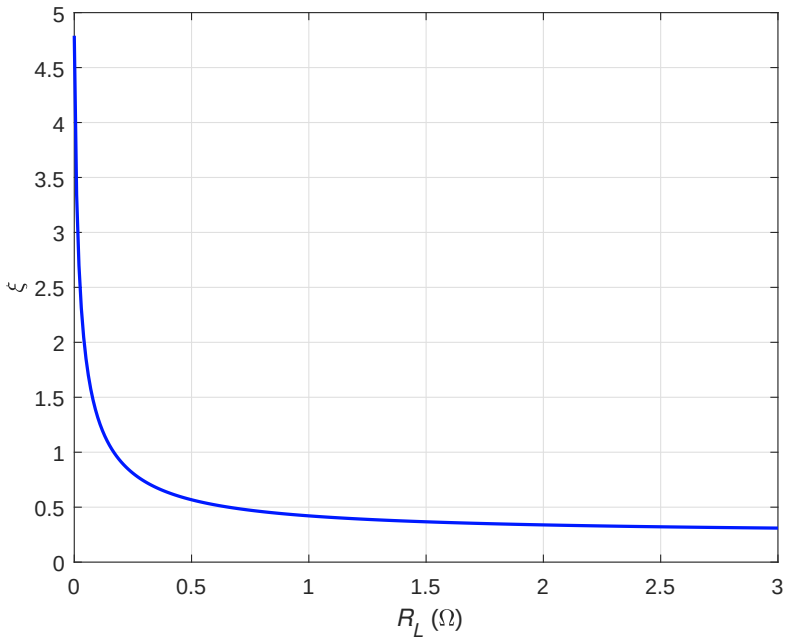

Figure 3.4: Damping factor ξ as a function of load resistance R_L.

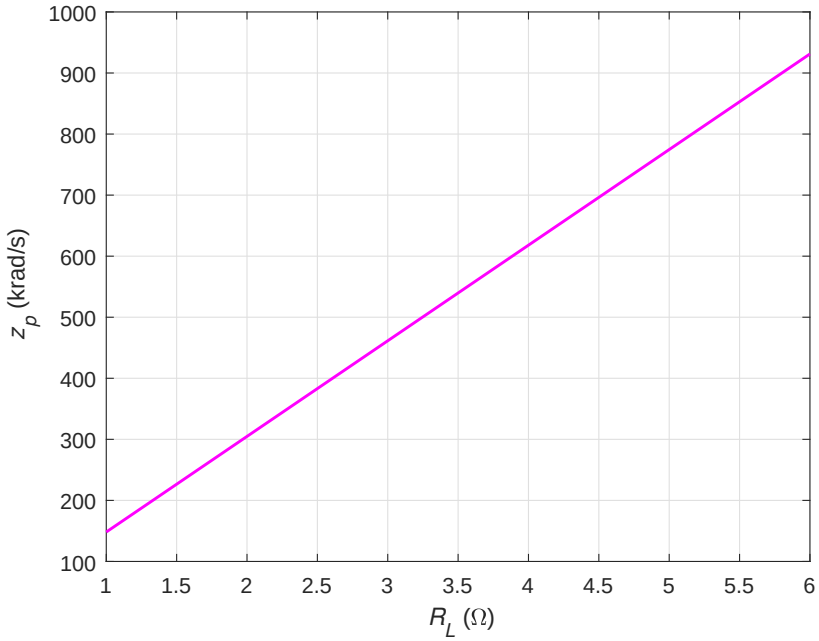

Figure 3.5: Location of RHP-zero z_p as a function of load resistance R_L.

Beyond $D > D_{cr}$, the RHP-zero shifts to the left-half of the s-plane.

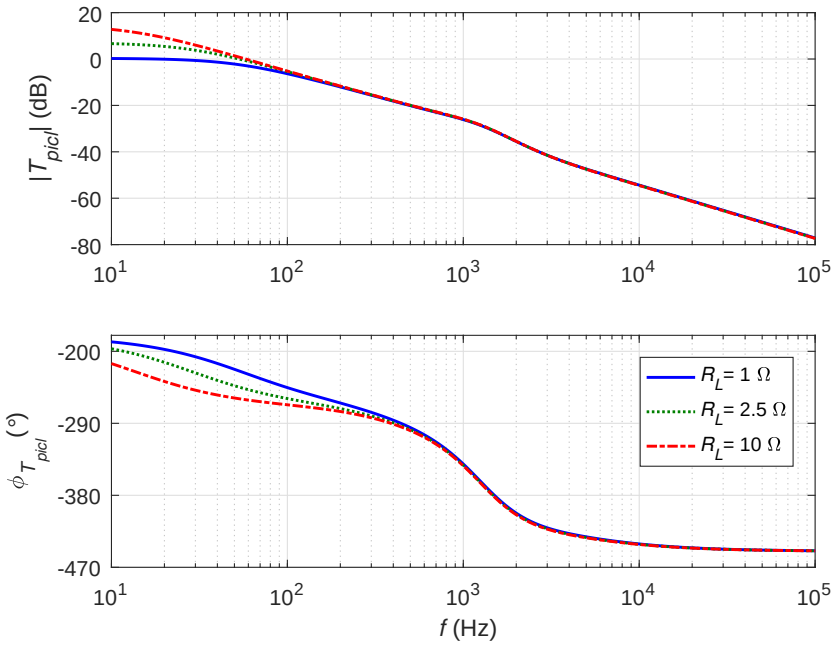

Figure 3.6: Magnitude and phase plots of the current-loop reference voltage-to-output voltage transfer function T_{picl} at selected values of load resistance for the buck-boost dc-dc converter.

3.2 Closed-Loop Characteristics

In this section, the transient responses of the open-loop, closed-inner loop, and closed-loop situations are analyzed and compared. The results of this section show the benefits of the closed-inner loop and closed-outer loop control. The results are discussed in the form of corresponding responses to step change in their input variables. The comparison is performed for the following systems:

- Open-loop power stage.
- Power stage with only closed-inner loop.
- Current-controlled power stage with outer-voltage loop.

Fig. 3.12 shows a comparison of the responses in output voltage of the buck-boost converter for a step change in the duty cycle by 0.1 unit for T_p and a step change in

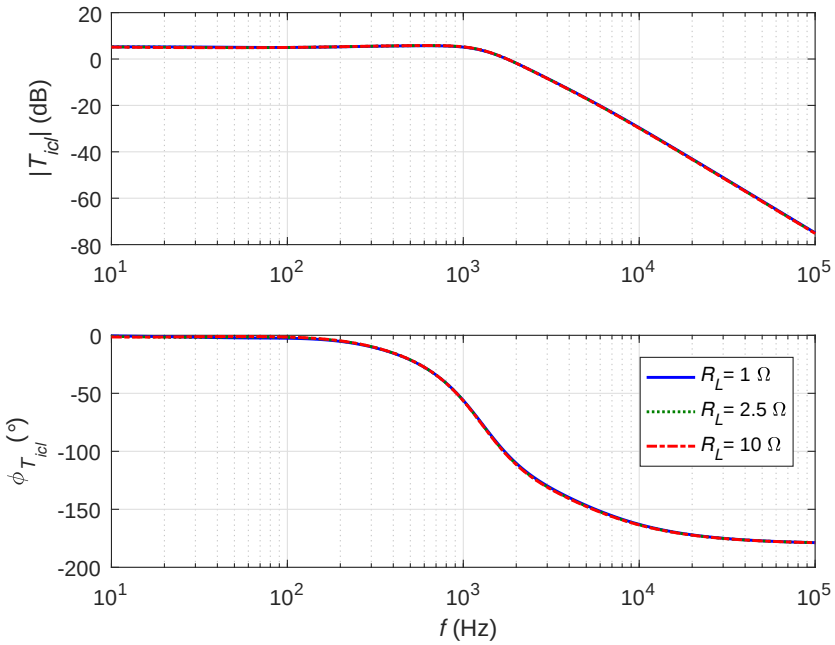

Figure 3.7: Magnitude and phase plots of the current-loop reference voltage-to-inductor current transfer function T_{icl} at selected values of load resistance for the buck-boost dc-dc converter.

the reference voltage by 1 V in T_{picl} and T_{pcl}. A major observation is the presence of the undershoot in the three step responses, which is a characteristic of converters with RHP zeros. The magnitude of undershoot is smaller in the closed-loop system, when compared to the open-loop transfer function T_p. A change in duty cycle by 0.1 unit corresponds to a change in the output voltage by nearly 2.25 V. A similar steady-state response can be observed for the T_{picl} transfer function, however, the response is slower than open-loop response. With the outer-voltage loop closed, an improved response to step change in the reference voltage can be observed. The output voltage changes by nearly 2 V and exhibits a short rise time and settling time characteristics. In conclusion, the response to output voltage is improved in the presence of a current-controlled power stage.

Fig. 3.13 shows a comparison of the responses in output voltage for a step change in the input voltage by 1 V in the power stage, current-controlled power stage, and

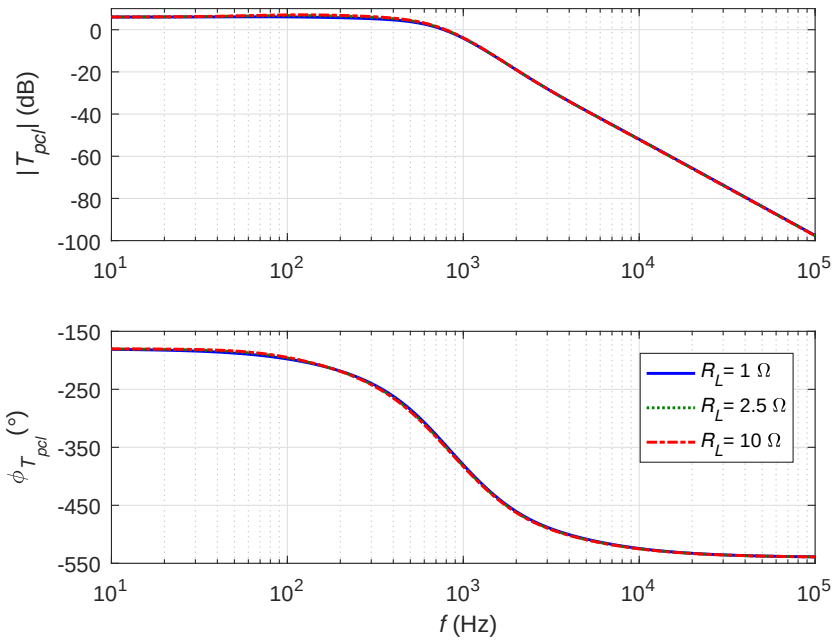

Figure 3.8: Magnitude and phase plots of the voltage-loop reference voltage-to-output voltage transfer function T_{pcl} at selected values of load resistance for the buck-boost dc-dc converter.

closed-outer loop. The input-to-output voltage transfer functions M_v, M_{vicl}, and M_{vcl} corresponding to the buck-boost power stage, power stage with only inner loop control, and buck-boost with both inner and outer loops are shown. The open-loop converter is highly susceptible to change in the input voltage. For example, for a 1 V change in the input voltage, the output voltage in an open-loop converter changes by nearly 0.4 V. However, for a 1 V change in the input voltage, the output voltage of the converter with only the inner loop increases only by nearly 100 mV. The inner current loop alone is not capable of providing 100% correction to changes in the input voltage. With the inclusion of the outer-voltage loop, the audio-susceptibility is further reduced significantly, where the output voltage is nearly unaffected by any change in the input voltage. Therefore, a two-loop control is the most suited topology for regulated power supplies.

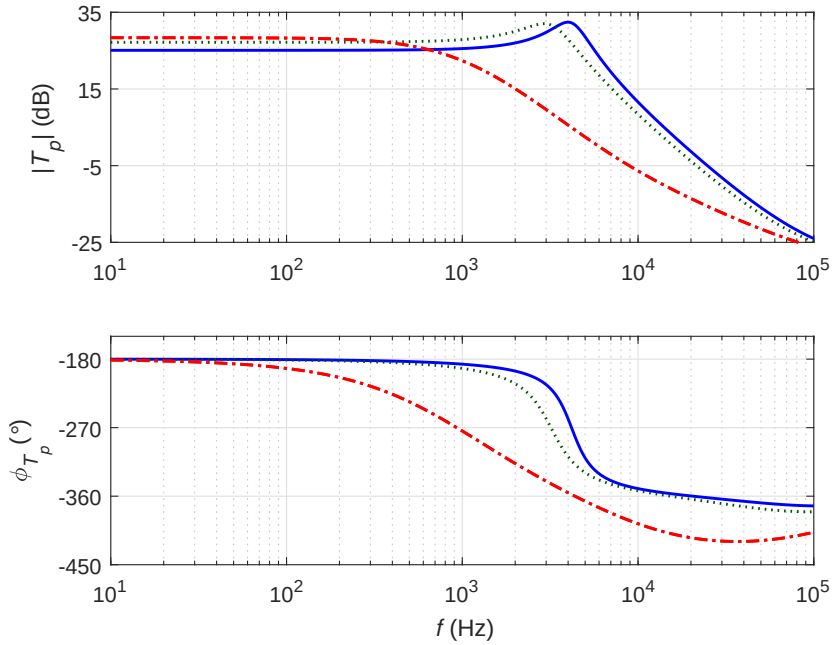

Figure 3.9: Magnitude and phase plots of the duty cycle-to-output voltage transfer function T_p at selected values of duty cycle for the buck-boost dc-dc converter.

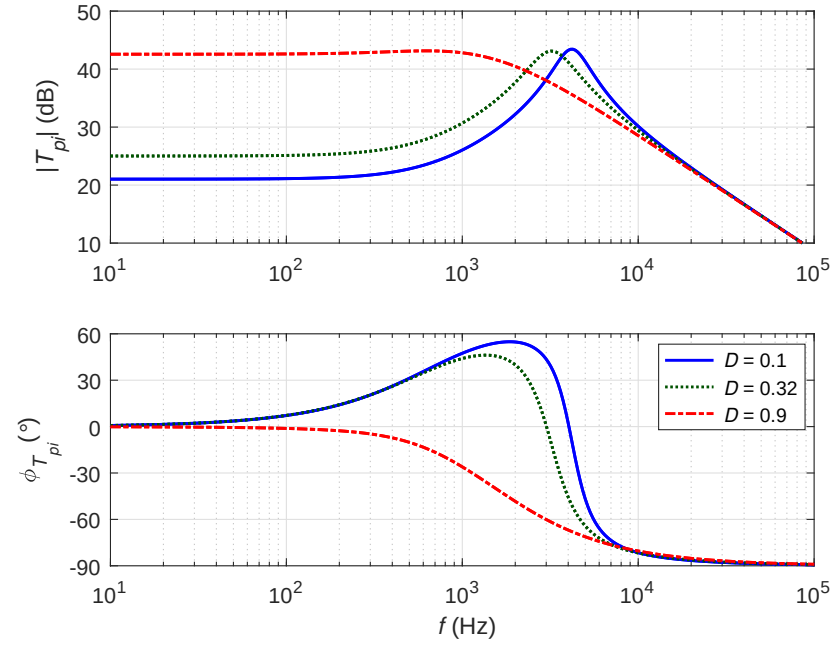

Figure 3.10: Magnitude and phase plots of the duty cycle-to-inductor current transfer function T_{pi} at selected values of duty cycle for the buck-boost dc-dc converter.

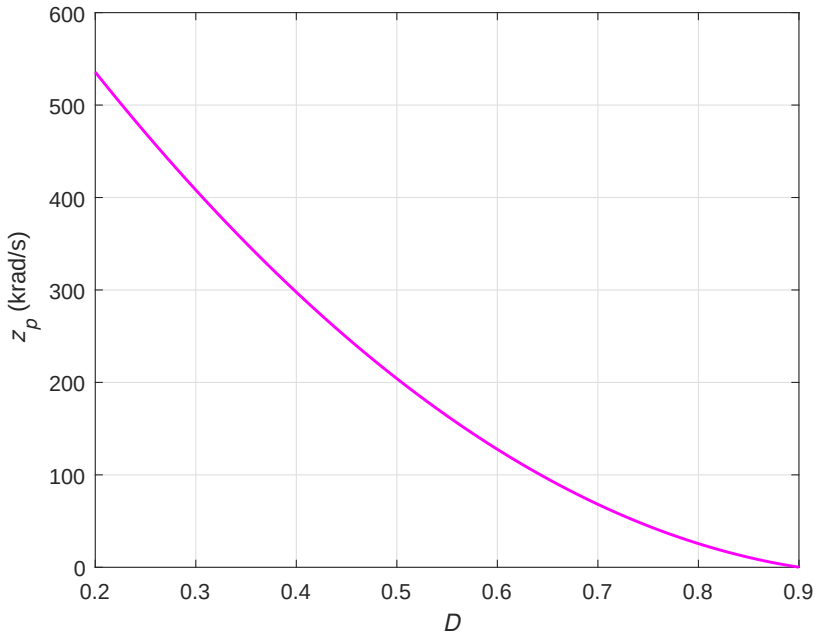

Figure 3.11: Location of RHP-zero z_p as a function of duty cycle D.

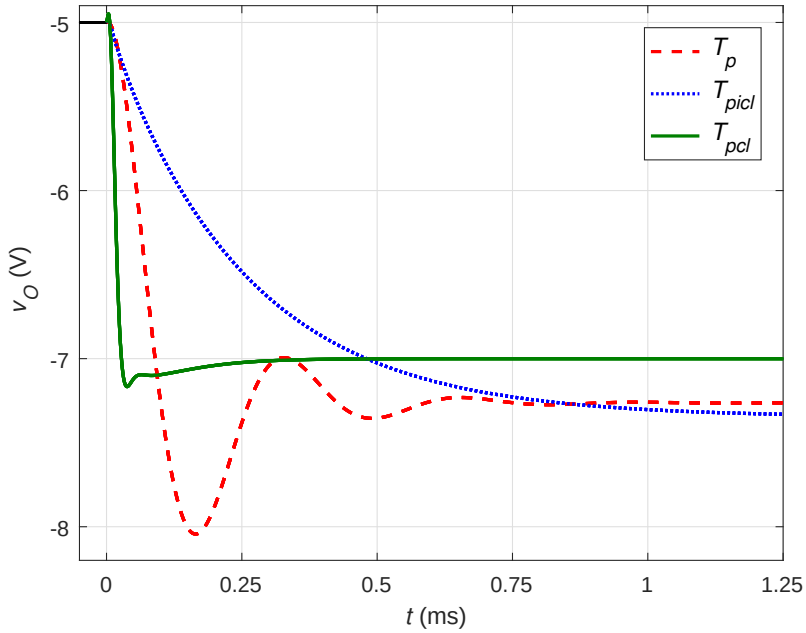

Figure 3.12: Comparison of responses in output voltages for step changes in duty cycle, current-loop reference, and voltage-loop reference voltages obtained using T_p, T_{picl}, and T_{pcl} transfer functions, respectively.

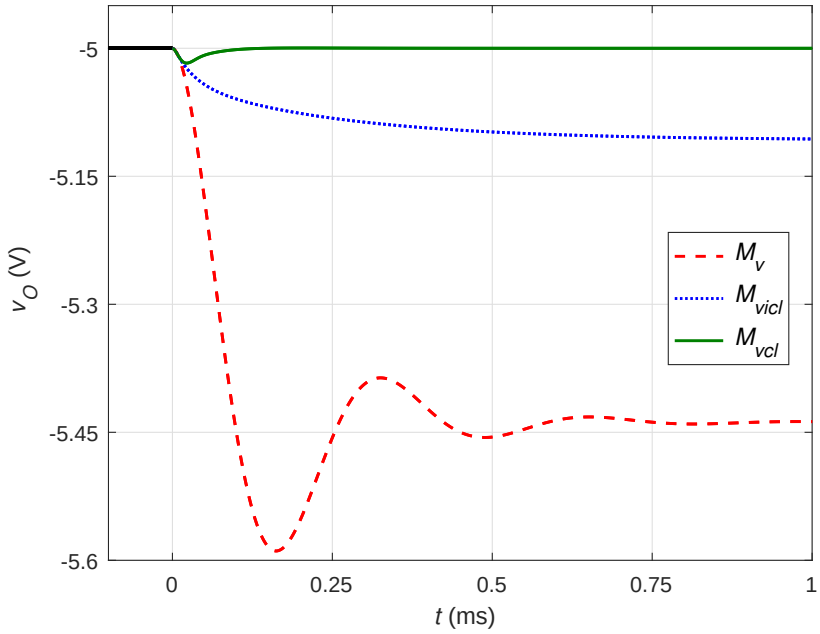

Figure 3.13: Comparison of responses in output voltages for step changes in input voltage by 1 V obtained using M_v, M_{vicl}, and M_{vcl} transfer functions, respectively.

Fig. 3.14 compares the ideal correction in duty cycle obtained using a dc model with that produced by closed-inner loop and outer-voltage loop for a step change in the input voltage by 1 V. Using the dc model, the exact correction in duty cycle required to maintain the output voltage constant is predicted using

$$\Delta D = -\left(\frac{1}{1+\eta\dfrac{V_I}{V_O}} + \frac{1}{1+\eta\dfrac{V_I+\Delta V_I}{V_O}}\right). \tag{3.3}$$

Therefore, for an output voltage $V_O = 5$ V, input voltage $V_I = 12$ V, efficiency of $\eta = 0.86$, and step change of $\Delta V_I = 1$ V, the change in duty cycle is $\Delta D = -0.0173$, i.e., the duty cycle must reduce from the initial value of $D = 0.321$ at $V_I = 12$ V to $D = 0.3037$ at $V_I = 13$ V. The reduction in duty cycle for change in input voltage must be produced by the two control loops. From Fig. 3.14, it can be seen that a majority of the correction in the duty cycle is provided by the inner loop. With only inner-current loop, the duty cycle can be reduced by nearly $\Delta D = 0.015$.

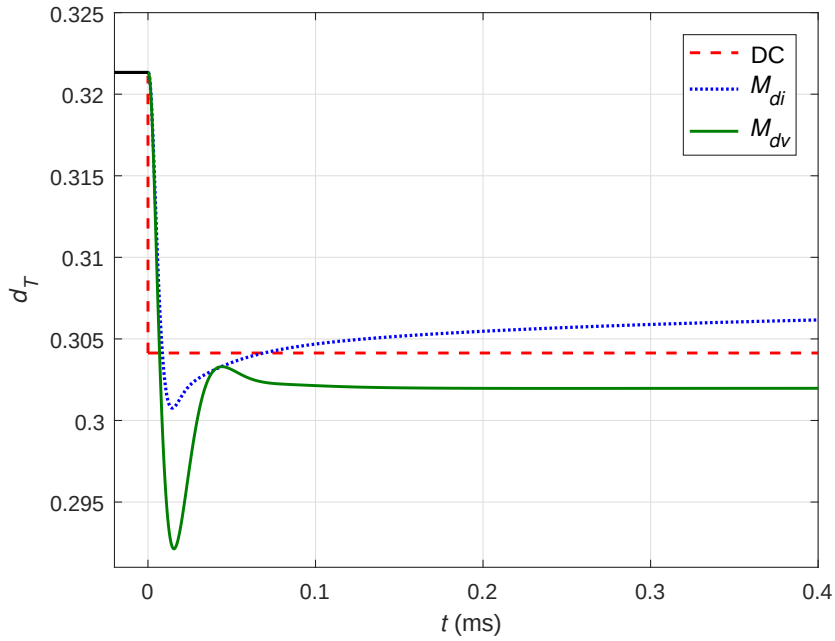

Figure 3.14: Comparison of responses in duty cycle for step changes in input voltage by 1 V.

The remaining correction is provided by the outer-voltage loop in order to achieve the desired response. Therefore, the current-controlled power stage has immense capabilities to counteract the input voltage disturbance with faster speed as well.

Fig. 3.15 shows the comparison of the responses in input current for step change in the input voltage for the open-loop, power stage with only closed-inner loop, and with two-loop controlled buck-boost dc-dc converter. In the dc-dc converter in open-loop configuration, the input current increases with increment in the input voltage. Therefore, the input impedance of an open-loop dc-dc converter offers a positive resistance effect at dc in accordance with Ohm's law. This can be observed in Fig. 3.16. In closed-loop dc-dc converter, with increase in the input voltage, the duty cycle must reduce to maintain a constant output voltage. As the duty cycle reduces, the switch S is ON for a smaller period of time, thereby reducing the input current. It can be seen in closed-loop converters, that with increase in input voltage, the input

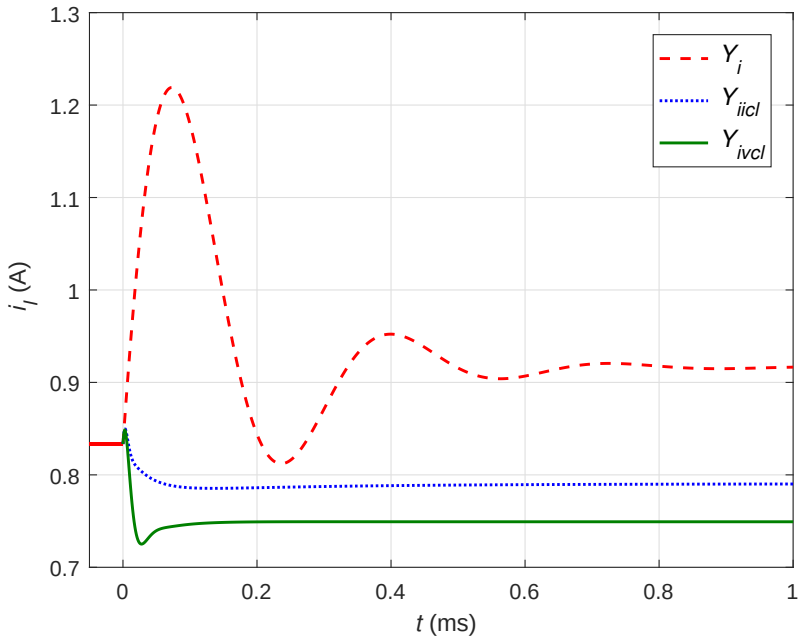

Figure 3.15: Comparison of the responses in input current for step change in the input voltage for the open-loop, power stage with only closed-inner loop, and with two-loop controlled buck-boost dc-dc converter.

current decreases, thereby creating a negative resistance at the input impedance of the converter implying an inverse Ohm's law phenomena. The negative resistance can be observed in both Figs. 3.17 and 3.18. The real part of the closed-loop impedances R_{iicl} and R_{ivcl} are negative at dc and low frequencies. The imaginary components or the input reactances X_{iicl} and X_{ivcl} are negligible at dc and low frequencies. For $f \geq f_s/10$, the input reactances are positive and show inductive properties. For frequencies $f > f_s/2$, the input reactance is capacitive. The range of zero reactance is wider in closed-loop converter than that in an open-loop converter.

Fig. 3.19 shows the comparison of responses in the output voltage for step change in the load current by 1 A for the open-loop, power stage with only closed-inner loop, and with two-loop controlled buck-boost dc-dc converter. In this analysis, it is assumed that a current source is placed across the load resistance, which injects current at the converter output node. In the open-loop dc-dc converter, the magnitude

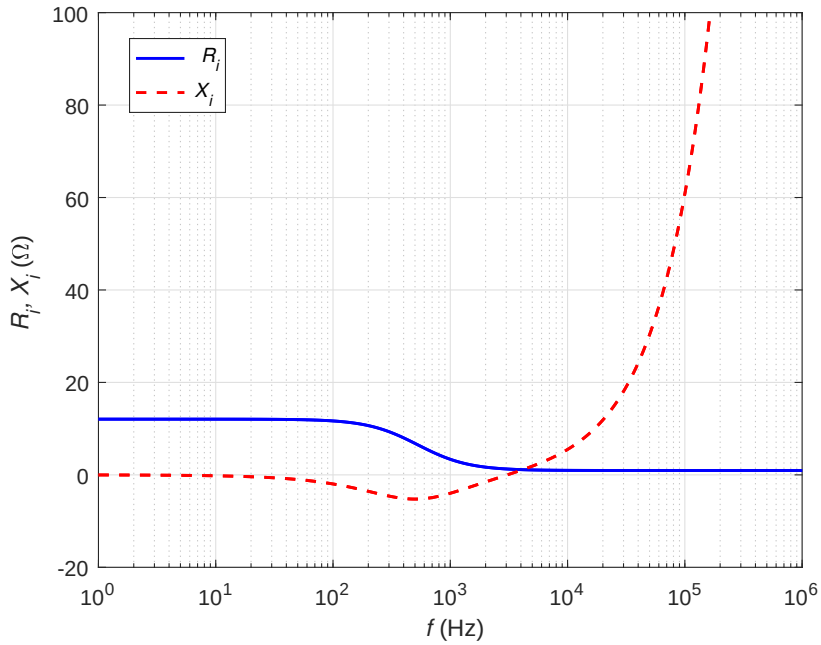

Figure 3.16: Real and imaginary components of the input impedance Z_i.

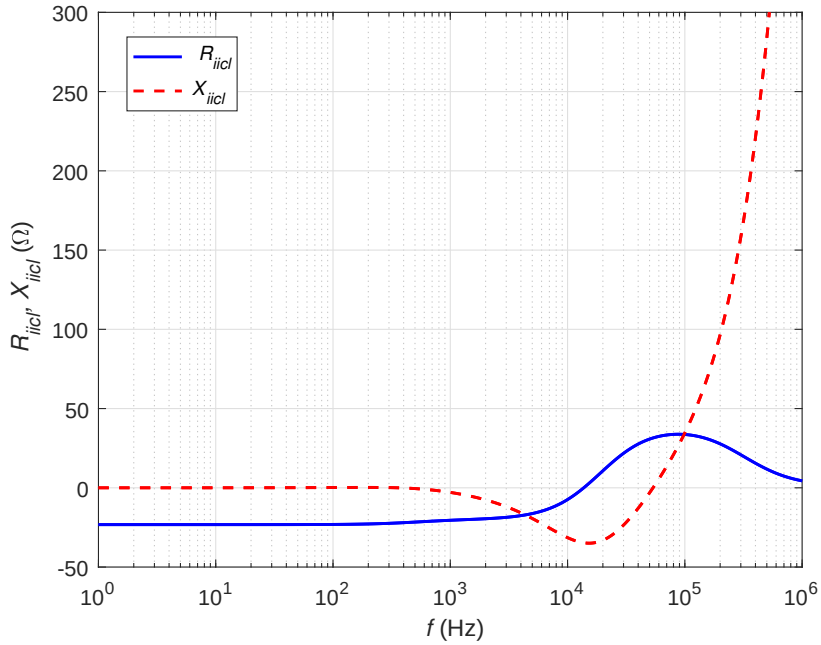

Figure 3.17: Real and imaginary components of the input impedance Z_{icl} with only closed-inner loop.

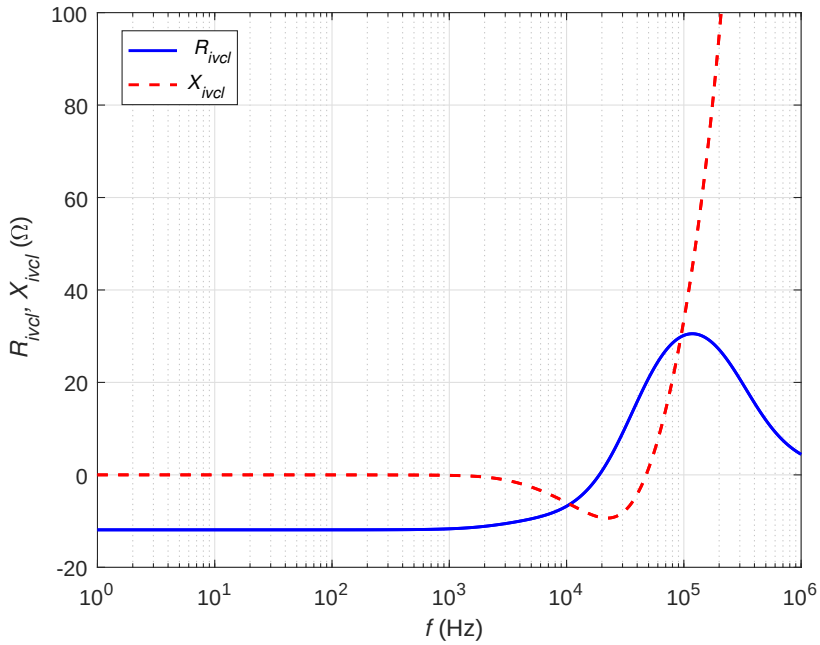

Figure 3.18: Real and imaginary components of the input impedance Z_{ivcl} with two-loop control.

of the output voltage increases with increase in the magnitude of the current. Fig. 3.20 shows the real and imaginary components of the open-loop output impedance Z_o. By ignoring the negative sign obtained due to current source effect, the open-loop output resistance is positive at dc and equal to $R_{o0} = 0.187\ \Omega$, i.e., for a change in the load current by 1 A, the output voltage increases by 0.187 V. Implementation of inner-current loop increases the magnitude of output resistance. Fig. 3.21 shows the real and imaginary components of the closed-loop output impedance Z_{oicl} with inner current loop. The magnitude of inner-current loop output resistance is $R_{oicl} = 1.932\ \Omega$, i.e., for a change in the load current by 1 A, the output voltage increases by 1.932 V. Fig. 3.22 shows the real and imaginary components of the output impedance Z_{ovcl} with outer-voltage loop. The outer-voltage loop decreases the output resistance $R_{ovcl} \approx 0$, i.e., for a change in the load current by 1 A, the output voltage remains unaffected and constant.

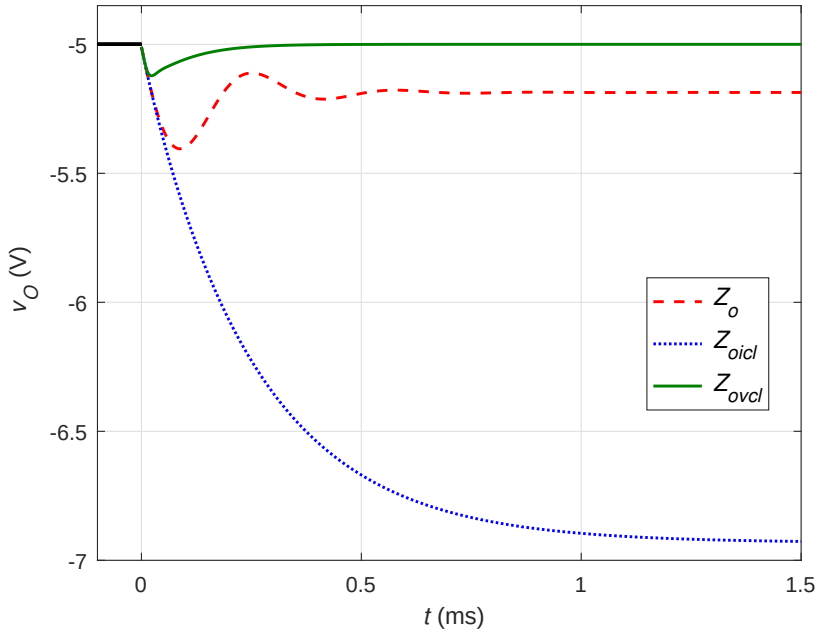

Figure 3.19: Comparison of responses in the output voltage for step changes in the load current by 1 A for the open-loop, power stage with only closed-inner loop, and with two-loop controlled buck-boost dc-dc converter.

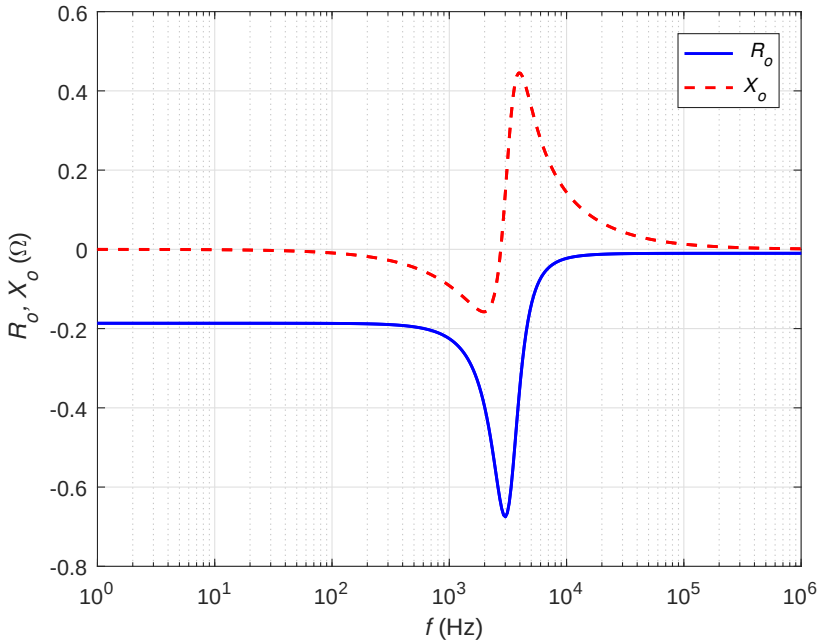

Figure 3.20: Real and imaginary components of the output impedance Z_o.

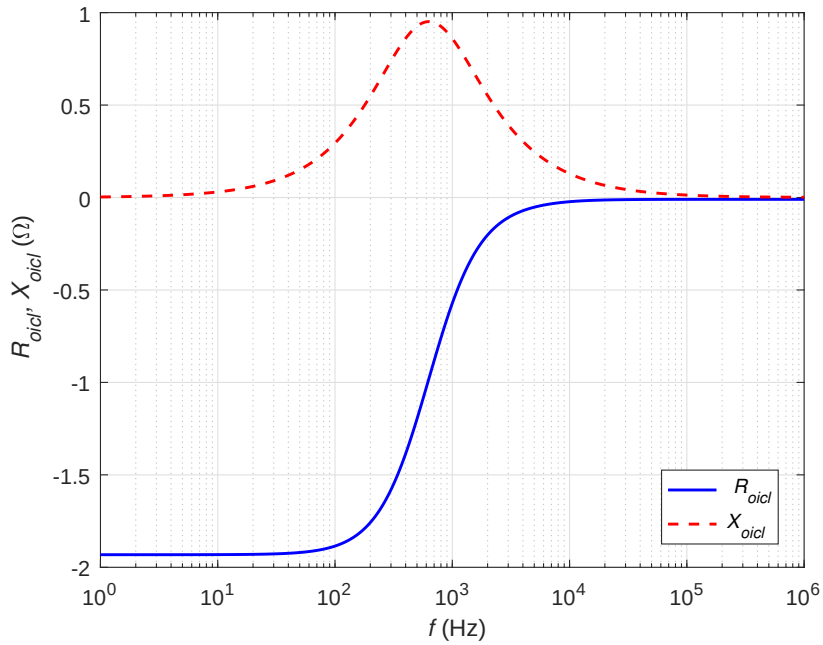

Figure 3.21: Real and imaginary components of the input impedance Z_{oicl} with only closed-inner loop.

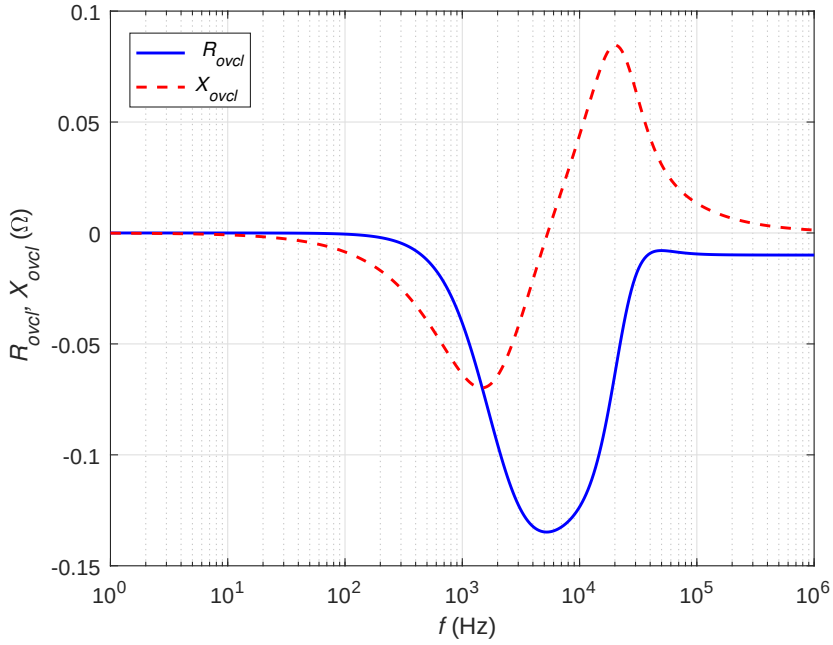

Figure 3.22: Real and imaginary components of the input impedance Z_{ovcl} with two-loop control.

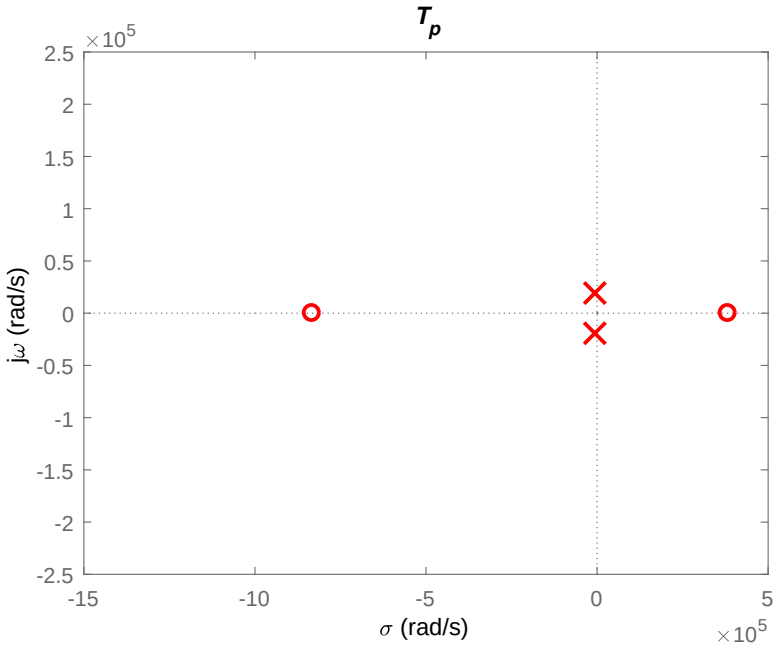

Figure 3.23: Pole-zero plot for the open-loop duty cycle-to-output voltage transfer function $T_p = v_o/d$.

3.2.1 Pole-Zero Analysis of Open-Loop and Closed-Loop Transfer Functions

In this section, the locations of poles and zeros for the open-loop and closed-loop transfer functions are presented. The relocation of the power stage and the introduction of new poles and zeros due to the inclusion of the inner-current loop and the outer-voltage loop are illustrated in the form of PZ-plots obtained using MATLAB. Only the control transfer functions are analyzed here as they are much critical for determining the converter stability.

Fig. 3.23 shows the pole-zero plot of the open-loop duty cycle-to-output voltage transfer function $T_p = v_o/d$. The following properties can be observed:

- It is a second order transfer function.
- A pair of complex conjugate poles located at undamped natural frequency f_o.

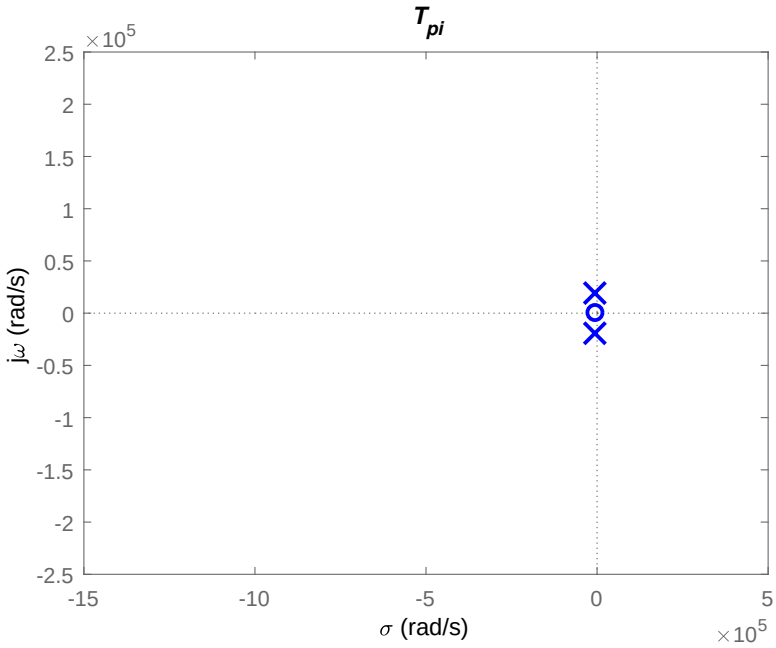

Figure 3.24: Pole-zero plot for the open-loop duty cycle-to-inductor current transfer function $T_{pi} = i_l/d$.

- Dominant pole effect is caused by complex conjugate poles located at f_o.
- One high-frequency right-half plane (RHP) zero f_{zp} and one very high-frequency left-half plane (LHP) zero f_{zn}.
- Power stage poles and zeros are fixed.

Fig. 3.24 shows the pole-zero plot of the open-loop duty cycle-to-inductor current transfer function $T_pi = i_l/d$. The following properties can be observed:

- It is a second order transfer function.
- A pair of complex conjugate located at undamped natural frequency f_o.
- Dominant pole effect is caused by a pole located at f_o.
- One low-frequency left-half plane (LHP) zero at f_{zi}.

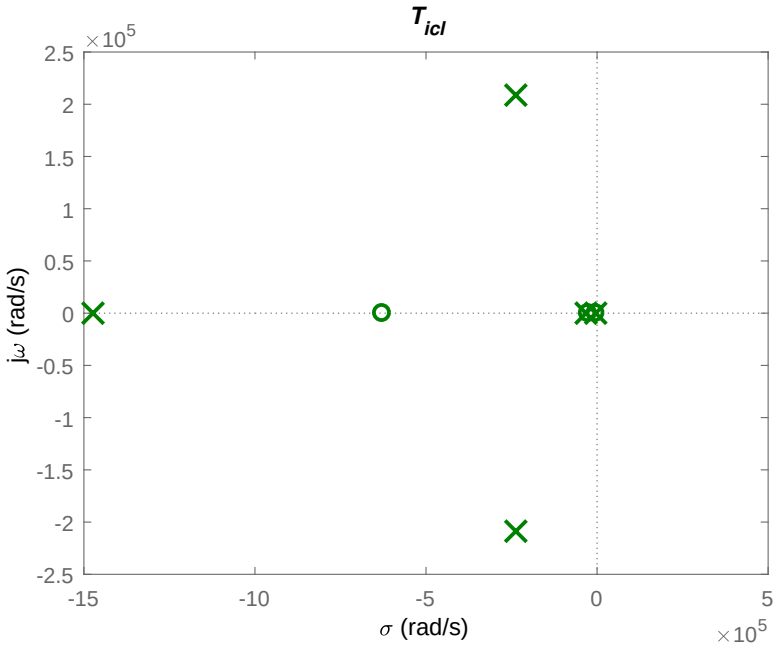

Figure 3.25: Pole-zero plot for the reference-to-inductor current transfer function $T_{icl} = i_l/v_{ri}$.

- Power stage poles and zeros are fixed.

Fig. 3.25 shows the pole-zero plot of the closed-loop current reference-to-inductor current transfer function $T_{icl} = i_l/v_{ri}$. The following properties can be observed:

- It is a fifth order transfer function.
- A pair of complex conjugate located at $f >> f_o$, one pole at origin by the controller, one pole at f_{pci} by the controller, one pole created by the low-pass filter in the feedback path.
- Dominant pole effect is caused by complex conjugate poles located at $f >> f_o$. Other low-frequency poles are nullified by corresponding zeros.
- One LHP low-frequency zero at f_{zi}, one LHP low-frequency zero by the controller at f_{zci}, and one LHP high-frequency zero.

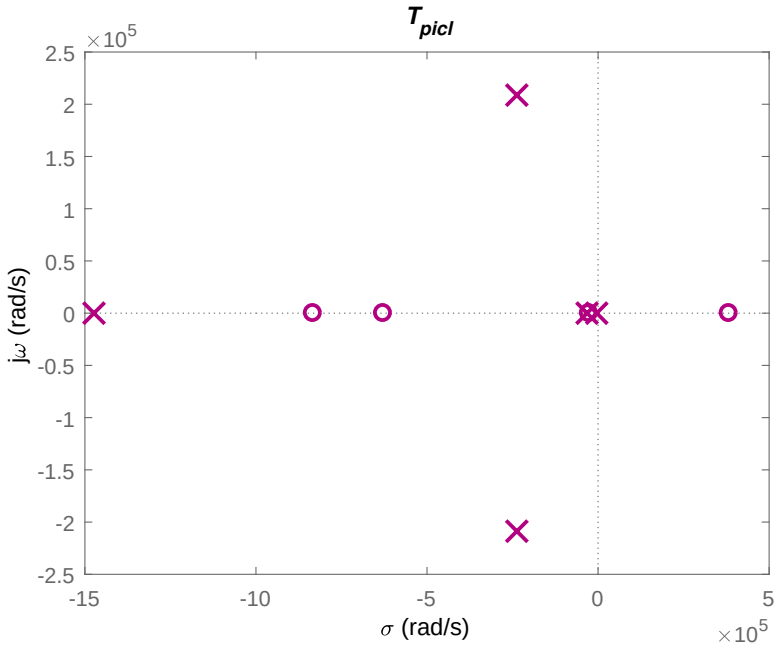

Figure 3.26: Pole-zero plot for the current reference-to-output voltage transfer function $T_{picl} = v_o/v_{ri}$.

- Complex pole pair at f_o has been relocated to a much higher frequency causing an increase in bandwidth.

Fig. 3.26 shows the pole-zero plot of the closed-loop current reference-to-inductor current transfer function $T_{picl} = v_o/v_{ri}$. The following properties can be observed:

- It is a fifth order transfer function.
- A pair of complex conjugate located at $f >> f_o$, one pole at origin by the controller, one pole at f_{pci} by the controller, one pole created by the low-pass filter in the feedback path.
- Dominant pole effect is caused by complex conjugate poles located at $f >> f_o$. Other low-frequency poles are nullified by corresponding zeros.
- One LHP low-frequency zero at f_{zi}, one LHP low-frequency zero by the controller at f_{zci}, one LHP very high-frequency zero at f_{zn}, one LHP high-frequency

zero, and one RHP zero located at f_{zp}.

- Complex pole pair at f_o has been relocated to a much higher frequency causing an increase in bandwidth. RHP zero is not relocated. Other poles and zero present in T_{icl} are not relocated.

Fig. 3.27 shows the pole-zero plot of the closed-loop current reference-to-inductor current transfer function $T_{pcl} = v_o/v_{rv}$. The following properties can be observed:

- It is a seventh order transfer function.
- Two pairs of complex conjugate located at $f >> f_o$, two LHP at low frequencies, one LHP at high frequency.
- Dominant pole effect is caused by complex conjugate poles located at $f >> f_o$. Other low-frequency poles are nullified by corresponding zeros. But the dominant pole is at a much lower frequency than that produced by the inner-current loop as seen in T_{icl}.
- One very high-frequency LHP zero at f_{zn}, one high-frequency LHP zero, one RHP zero located at f_{zp}, two LHP zeros at very low frequencies.
- A complex pole pair at f_o has been relocated to a much higher frequency. New pair of complex pole has been created close to f_o causing a reduction in bandwidth of outer-voltage loop. RHP zero is not relocated.

Fig. 3.28 shows the trajectory of the poles and zeros of the duty cycle-to-output voltage transfer function T_p obtained at selected values of the load resistance R_L. The zero z_n caused by the filter capacitor C and its equivalent series resistance r_C do not move with the load resistance as it is independent of the load resistance. The location of the poles p_1, p_2 is not affected by the load resistance. A clearer illustration of the movement can be observed in Fig. 3.29. However, the RHP zero z_p moves towards

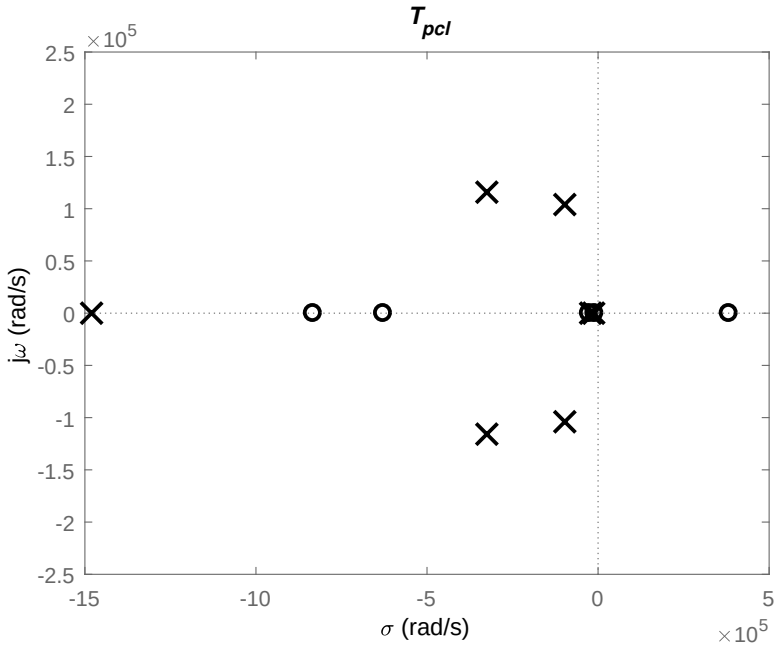

Figure 3.27: Pole-zero plot for the voltage reference-to-output voltage transfer function $T_{pcl} = v_o/v_{rv}$.

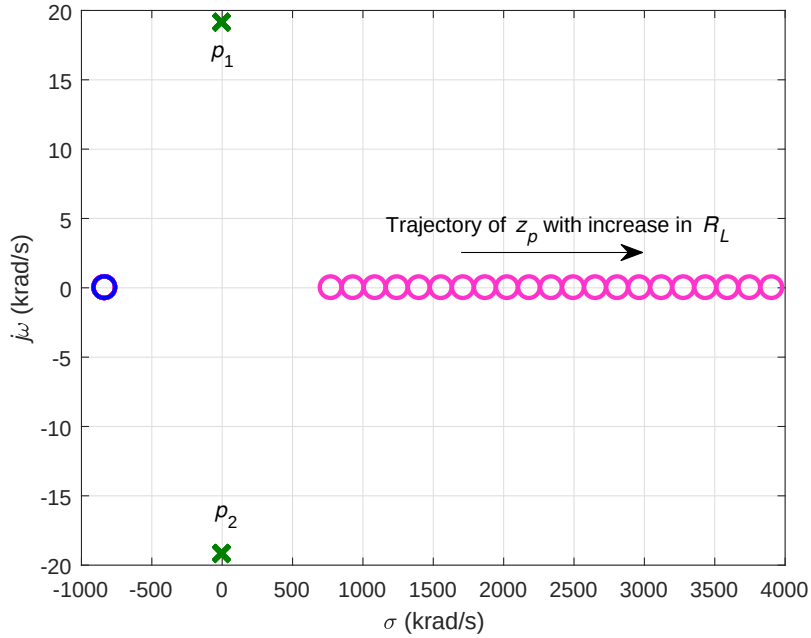

Figure 3.28: Trajectory of poles and zeros of the open-loop duty cycle-to-output voltage transfer function as functions of the load resistance.

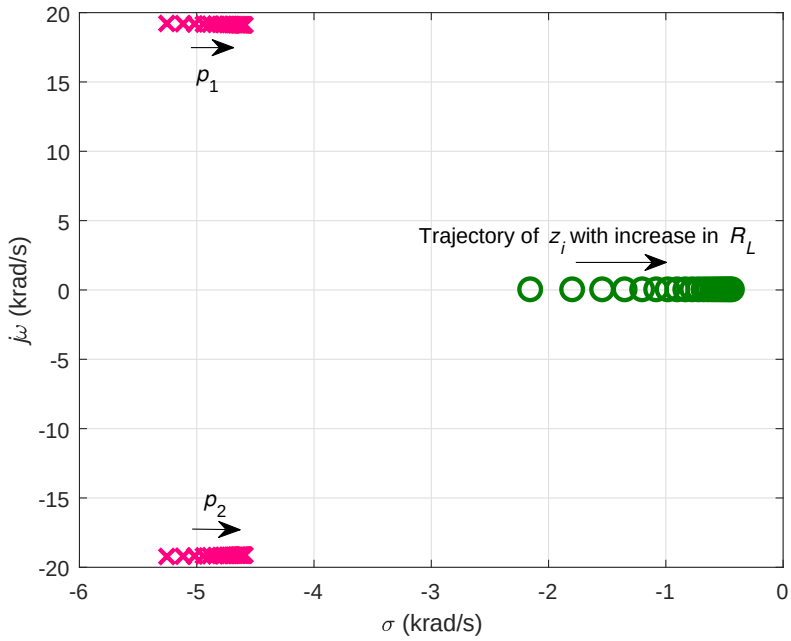

Figure 3.29: Trajectory of poles and zeros of the open-loop duty cycle-to-inductor current transfer function as functions of the load resistance.

∞ with increase in the load resistance. This means that the converter stability is much larger at high load resistance or low output power. This plot indicates that the controller for the power-stage must be designed for the worst-case condition occurring at a minimum load resistance. Fig. 3.29 shows the trajectory of the poles and zeros of the duty cycle-to-inductor current transfer function T_{pi} obtained at selected values of the load resistance R_L. One may clearly observe that the location of the poles p_1 and p_2 is not impacted by the variation in load resistance over the desired range. However, the low-frequency LHP zero z_i moves towards the origin with increase in load resistance. From the design point-of-view, the controller for the current loop must be designed for the maximum load resistance specifications or minimum output power.

Fig. 3.30 shows the trajectory of the poles and zeros of the duty cycle-to-output voltage transfer function T_p obtained at selected values of the duty cycle D. The zero

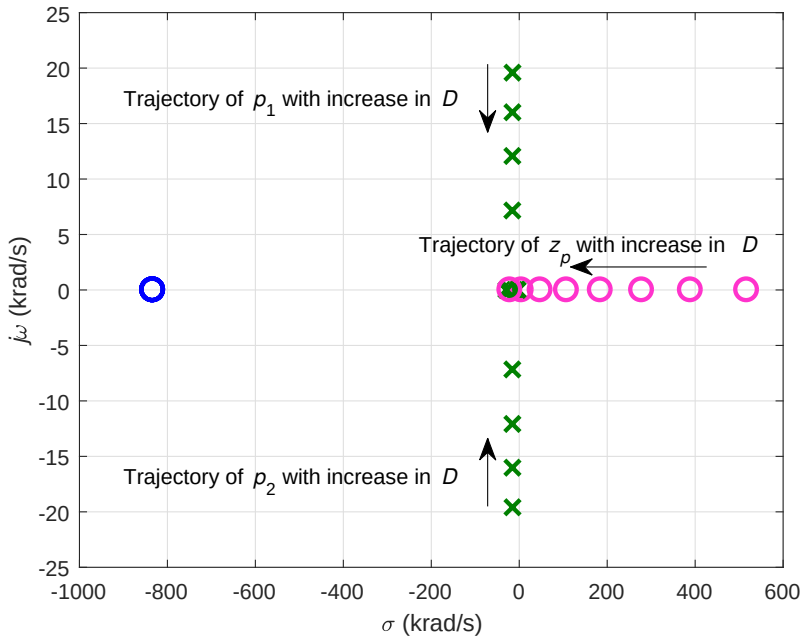

Figure 3.30: Trajectory of poles and zeros of the open-loop duty cycle-to-output voltage transfer function as functions of the duty cycle.

z_n caused by the filter capacitor C and its equivalent series resistance r_C do not move with the duty cycle as it is independent of the duty cycle. The location of the poles p_1, p_2 is severely affected by the duty cycle. A clearer illustration of the movement can be observed in Fig. 3.31. The RHP zero moves towards the origin with increase in the duty cycle. At low duty ratios, the zero is located in the right-half of the s-plane. With increase in the duty cycle, the RHP-zero moves towards the origin. At $R_L(1-D)^2 = r$, the RHP zero is at the origin. This corresponds to a critical duty cycle determined by

$$D_{cr} = 1 - \sqrt{\frac{r}{R_L}}. \tag{3.4}$$

Beyond $D > D_{cr}$, the RHP-zero shifts to the left-half of the s-plane.

The zero z_i is independent of the duty cycle. The poles p_1, p_2 are severely affected by the change in duty cycle. The location of the real component of the poles p_1, p_2 marginally moves towards $-\infty$. The imaginary component the poles p_1, p_2 reduces

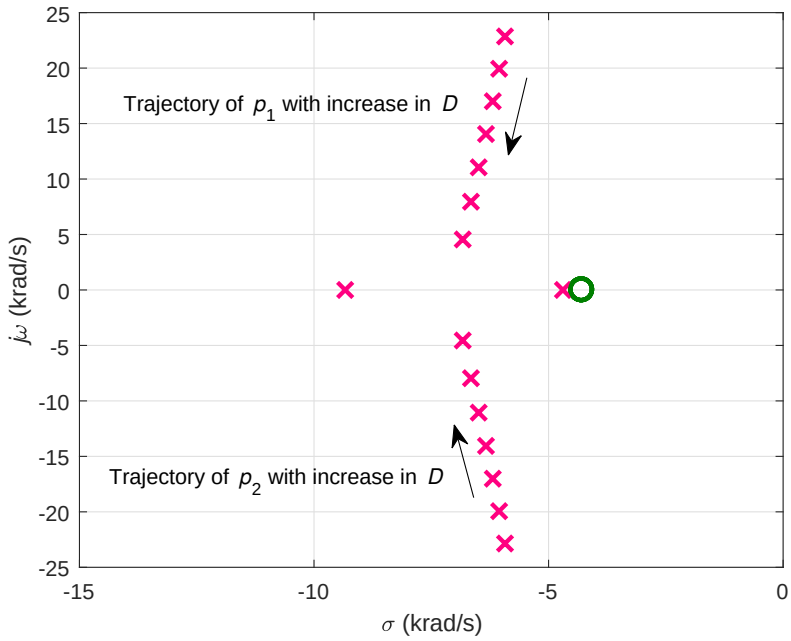

Figure 3.31: Trajectory of poles and zeros of the open-loop duty cycle-to-inductor current transfer function as functions of the duty cycle.

with increase in duty cycle. Beyond a critical duty cycle, the imaginary component of the poles meet the real axis and are transformed into real poles. The pole p_1 moves towards $-\infty$ while the pole p_2 moves towards the origin with increase in the duty cycle beyond a critical value.

3.3 Design of Buck-Boost Prototype for Experiments

A buck-boost converter was designed, built, and tested for the following specifications: supply voltage $V_I = 12$ V, output voltage $V_O = -5$ V, and switching frequency $f_s = 200$ kHz. The selected load resistance was $R_L = 3\ \Omega$. The inductance to ensure CCM was $L = 10\ \mu$H and filter capacitance was $C = 100\ \mu$F. The selected MOSFET was IRF540 by International Rectifiers and the selected diode was MBR10100 by Vishay Semiconductors. The required duty cycle to achieve the rated output voltage was $D = 0.37$. The equivalent averaged resistance was $r \approx 0.4\ \Omega$. A buck-boost converter satisfying the design constraints was built. The inductor was built on a

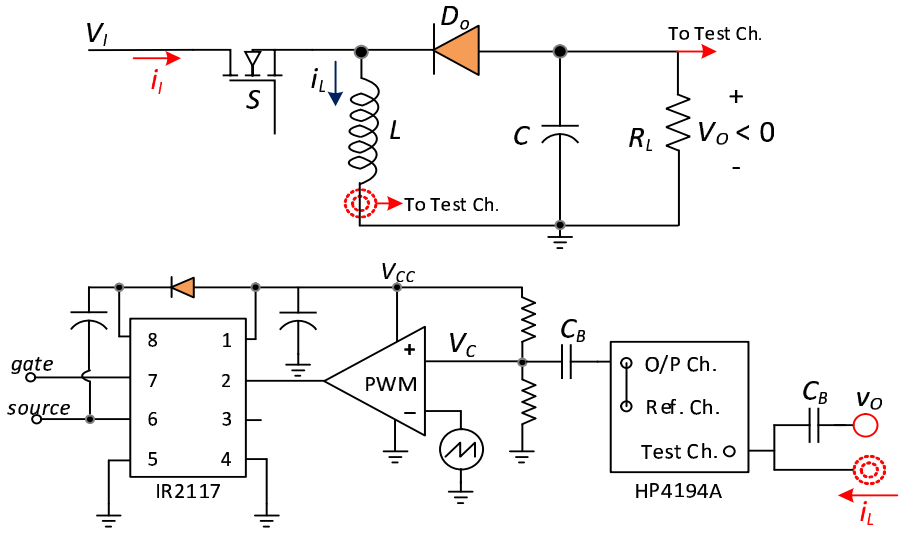

Figure 3.32: Experimental set-up to measure the control path transfer functions.

ferrite pot-core with an air-gap 0f 0.25 mm. The measured inductance was $L = 18\ \mu$H and the equivalent series resistance was $r_L = 0.12\ \Omega$. The electrolytic capacitor used was $C = 100\ \mu$F and the equivalent series resistance was $r_C = 0.3\ \Omega$. The dc output current and the average inductor current were $I_O = 1.67$ A and $I_L = I_O/(1 - D) = 2.65$ A, respectively. The selected sense resistor was $R_s = 0.7\ \Omega$ to yield the dc reference voltage as $V_{RI} = I_L R_s = 1.87$ V.

3.4 Power-Stage Transfer Functions

The power-stage transfer functions were analyzed for the converter specifications and design provided in Section 3.3. An experimental prototype of the buck-boost converter was built, measured, and tested. An HP4194A gain-phase analyzer was used to obtain the Bode plots for the described transfer functions. Pearson 411 wide-bandwidth current transformer with a gain 0.1 A/V $= -20$ dB was used to record the inductor current. DC blocking capacitors of value $C_B = 47\ \mu$F with negligible series resistances were used at the small-signal voltage injection and extraction nodes. A modulator gain $T_m = -13.79$ dB was added to the measurement data of T_p and T_{pi}. The

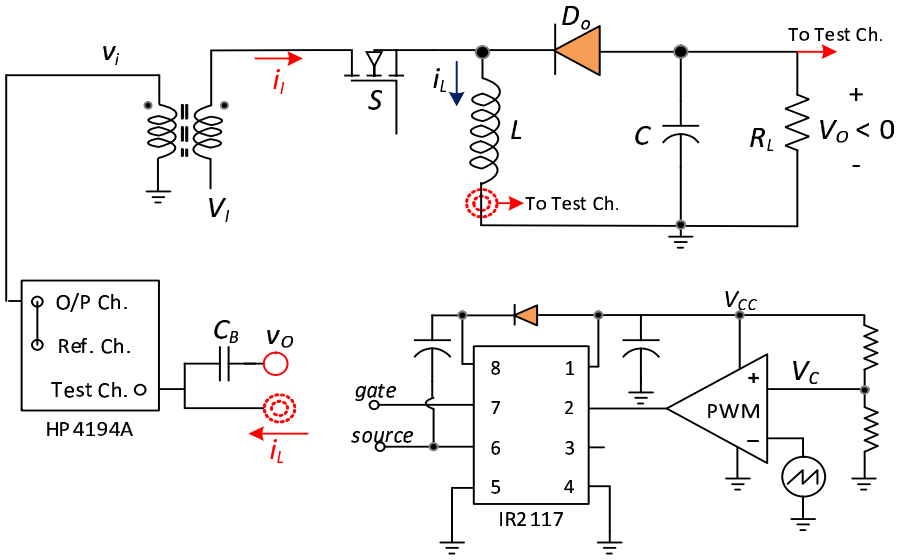

Figure 3.33: Experimental set-up to measure the disturbance path transfer functions.

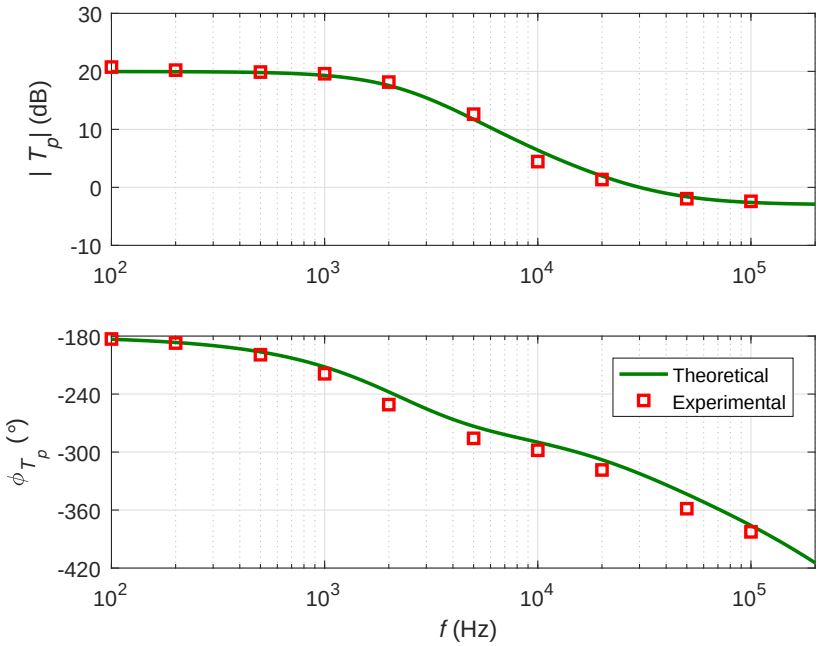

Figure 3.34: Experimental validation of theoretically obtained duty cycle-to-output voltage transfer function T_p.

current-probe compensation of -20 dB was added to T_{pi}. All the transfer functions are derived and given in Chapter 2. The experimental set-up to measure the transfer functions T_p and T_{pi} is as shown in Fig. 3.32.

Fig. 3.34 shows the theoretical and experimental magnitude and phase plots of the duty-to-output voltage transfer function T_p. The following parameters were obtained: gain at dc $T_{po} = 25.24$ dB $= 18.29$ V/V, right-half plane (RHP) zero $f_{zp} = \omega_{zp}/2\pi = 32.23$ kHz, LHP zero $f_{zn} = \omega_{zn}/2\pi = 5.3$ kHz. The complex-conjugate poles are same for both T_{pi} and T_p transfer functions, given by $p_1, p_2 = -16.3 \pm 8.15$ krad/s. The change in the phase shift of T_p transfer function exceeds $-180°$, which requires a higher order controller for the outer loop.

In the experimental verification, a time delay T_d is observed from the input of the network analyzer to the duty cycle caused by the pulse-width modulator, gate-driver, and the MOSFET. The delay was measured as $T_d = 1$ μs for the apparatus used in the experiments. The time delay the frequency spectrum between dc and $f_s/2$ is equal to e^{-sT_d} and is approximated using first-order Padè function as [21]

$$e^{-sT_d} \approx= \frac{1 - s\frac{T_d}{2}}{1 + s\frac{T_d}{2}} = -\frac{s - \frac{2}{T_d}}{s + \frac{2}{T_d}} \tag{3.5}$$

to yield the modified expression for the duty cycle-to-output voltage transfer function as

$$T_p(s) = \frac{v_o(s)}{d(s)} = -T_{px}\frac{(s + \omega_{zn})(s - \omega_{zp})}{s^2 + 2\xi\omega_0 s + \omega_0^2}\frac{s - \frac{2}{T_d}}{s + \frac{2}{T_d}} \tag{3.6}$$

The Padè approximation was included in the theoretical analysis. The magnitude plot is unaffected. An excellent agreement between the theoretical and experimental results was observed.

Fig. 3.35 compares the theoretically and experimentally obtained magnitude and phase plots of the duty cycle-to-inductor current transfer function T_{pi}. The following frequency-domain parameters were obtained: low-frequency left-half plane (LHP) zero natural corner frequency $f_o = \omega_o/2\pi = 2.6$ kHz, $f_{zi} = \omega_{zi}/2\pi = 639.23$ Hz, damping factor $\xi = 0.9472$, and gain at dc $T_{pio} = 22.85$ dB $= 13.88$ V/V. The low-frequency LHP zero was at $\omega_{zi} = 4.02$ krad/s. The complex-conjugate poles of T_{pi} transfer

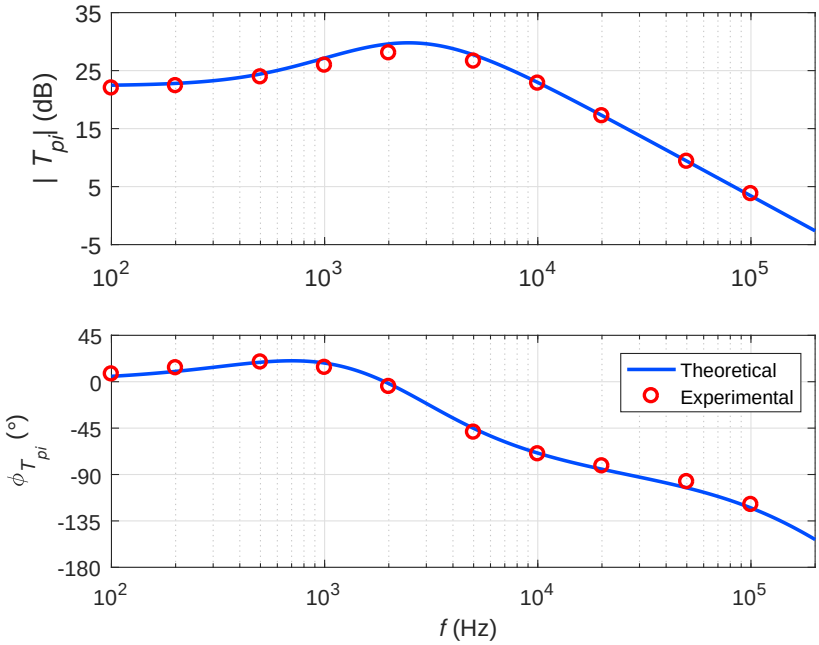

Figure 3.35: Experimental validation of theoretically obtained duty cycle-to-inductor current transfer function T_{pi}.

functions were $p_1, p_2 = -16.3 \pm 8.15$ krad/s. Since ω_{zi} is lower than the real part of the complex-conjugate poles, the low-frequency zero compensate one of the complex poles. Therefore, neglecting the delay, the phase does not decrease below $-90°$ and is positive at low frequencies. This makes the compensation of the outer loop much easier.

The Padé approximation was included in the theoretical analysis. The magnitude plot is unaffected. An excellent agreement between the theoretical and experimental results was observed. The experimental set-up to measure the transfer functions M_v, M_{vi}, and Z_i is as shown in Fig. 3.33. Fig. 3.36 shows the experimental and theoretical results of the input-to-output voltage transfer function M_v. A small-signal voltage variation was introduced in series with the dc supply voltage by means of a p-channel power transistor operating in the active region. An isolation transformer SD250 was used to drive the gate and source terminals of the p-channel transistor. The voltage

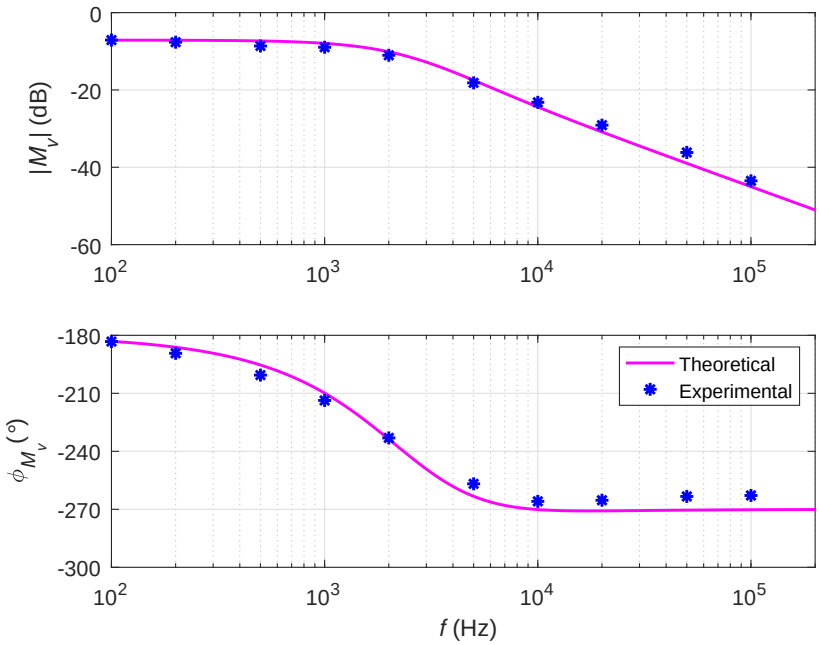

Figure 3.36: Experimental validation of theoretically obtained input-to-output transfer function M_v.

gain of the additional circuitry was measured using the network analyzer and then added to the measurement data.

Fig. 3.37 shows the experimental and theoretical results of the input voltage-to-inductor current transfer function M_{vi}. A small-signal voltage variation was introduced in series with the dc supply voltage by means of a p-channel power transistor operating in the active region. An isolation transformer SD250 was used to drive the gate and source terminals of the p-channel transistor. The voltage gain of the additional circuitry was measured using the network analyzer and then added to the measurement data. A compensation of -20 dB was added to account for the gain of the Pearson current probe. The gain at dc and low-frequencies is nearly $M_{vi0} = -12.46$ dB $= 0.2382$ V/V. The low-frequency left-half plane zero (LHP) zero is $f_{zvi} = \omega_{zvi}/2\pi = 482$ Hz. A good agreement between theoretical and experimental data was observed.

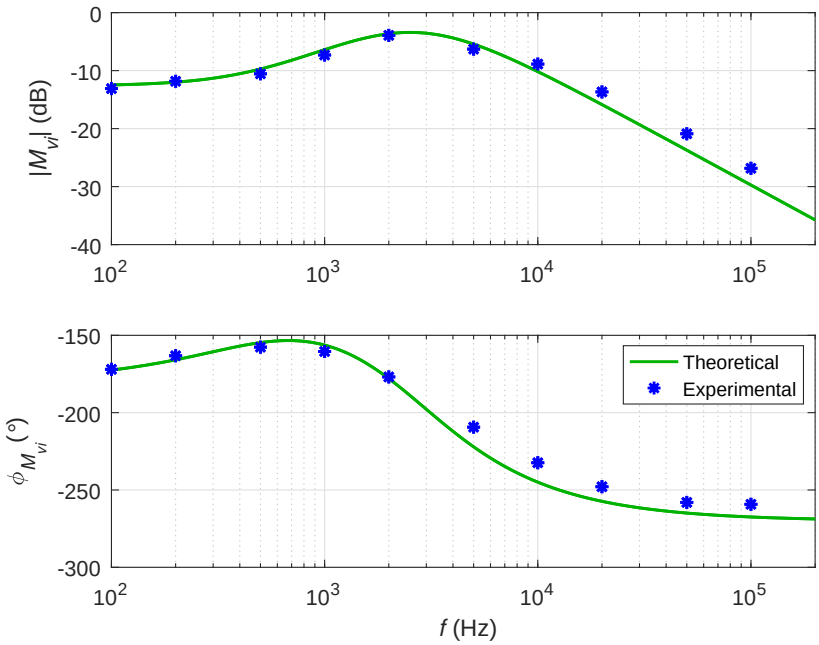

Figure 3.37: Experimental validation of theoretically obtained input voltage-to-inductor current transfer function M_{vi}.

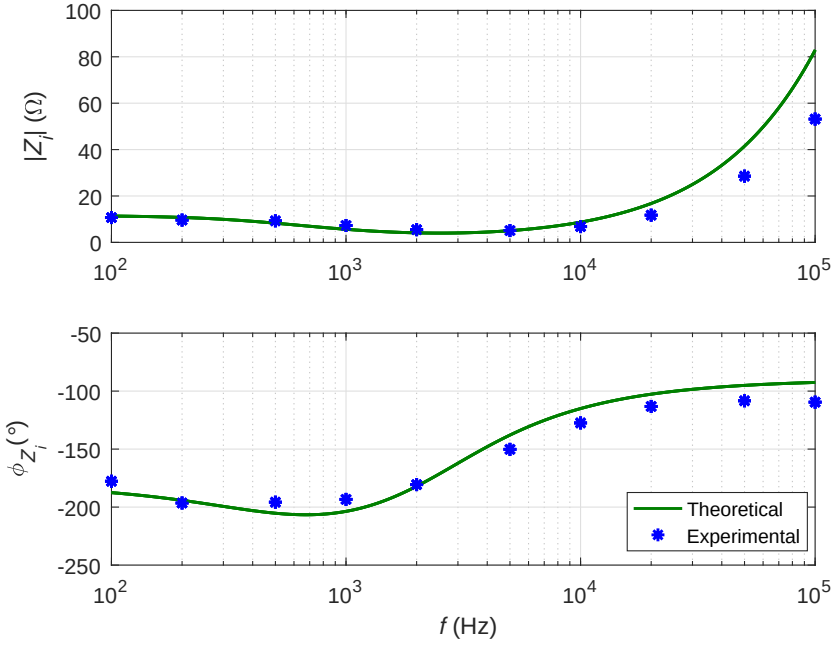

Figure 3.38: Experimental validation of theoretically obtained output voltage-to-output current transfer function Z_i.

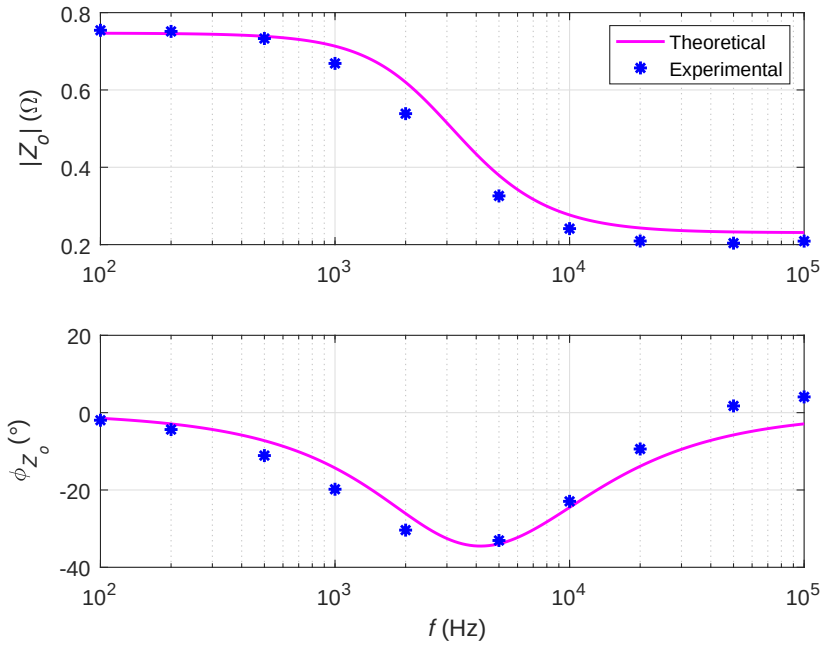

Figure 3.39: Experimental validation of theoretically obtained input voltage-to-input current transfer function Z_o.

Fig. 3.38 shows the experimental and theoretical results of the input impedance Z_i. A small-signal voltage variation was introduced in series with the dc supply voltage by means of a p-channel power transistor operating in the active region. An isolation transformer SD250 was used to drive the gate and source terminals of the p-channel transistor. The voltage gain of the additional circuitry was measured using the network analyzer and then added to the measurement data. A compensation of -20 dB was added to account for the gain of the Pearson current probe. A good agreement between theoretical and experimental data was observed.

Fig. 3.39 shows the experimental and theoretical results of the output impedance Z_o. A small-signal voltage perturbation was introduced through the injection transformer SD250 connected across the load resistor. A dc blocking capacitor C_B was used in series with the primary winding of the transformer to prevent the flow of dc current into the small-signal ac voltage source. A compensation of -20 dB was added

to account for the gain of the Pearson current probe. A good agreement between theoretical and experimental data was observed.

3.5 Transfer Functions of Closed-Inner Current Loop

The transfer function of the pulse-width modulator is [34]

$$T_m = \frac{1}{V_{Tm}}, \tag{3.7}$$

where V_{Tm} is the maximum value of the saw-tooth waveform. In this work, $V_{Tm} = 5$ V. The gain of the pulse-width modulator is therefore, $T_m = 1/V_{Tm} = 0.2 = -13.79$ dB. The transfer function of the low-pass filter is

$$T_f = \frac{1}{1 + \frac{s}{\omega_{pf}}}, \tag{3.8}$$

where $f_{pf} = \omega_{pf}/2\pi = 1/(R_f C_f)$ is the upper cutoff frequency. The cutoff frequency of the low-pass filter can be selected based on the maximum allowable feedback voltage ripple. By expressing (3.8) in frequency domain, the magnitude of T_f at the switching frequency is

$$|T_f(f_s)| = \frac{\Delta v_{FI}}{\Delta v_{Rs}} = \frac{1}{\sqrt{1 + \left(\frac{f_s}{f_{pf}}\right)^2}} \tag{3.9}$$

to yield the upper cutoff frequency as

$$f_{pf} = \sqrt{\frac{1}{\left(\frac{\Delta v_{Rs}}{\Delta v_{FI}}\right)^2 - 1}} f_s = \frac{1}{2\pi R_f C_f}. \tag{3.10}$$

Assuming a maximum allowable ripple ratio $\Delta v_{FI}/\Delta v_{Rs} = 40\%$ at the switching frequency $f_s = 200$ kHz yields the filter upper cutoff frequency as $f_{pf} = 100$ kHz. A standard resistor $R_f = 1$ kΩ was selected leading to a filter capacitance was $C_f = 1.59$ nF. A standard 1.8 nF capacitor was used.

3.6 Loop Gain

Appropriate selection of current-loop controller is made by evaluating the characteristics of the uncompensated loop gain T_{ki}. The uncompensated loop gain is

$$T_{ki} = \frac{v_{ei}}{v_{fi}} = T_m T_{pi} R_s T_f. \tag{3.11}$$

Fig. 2.22 in Chapter 2 shows the Bode magnitude and phase of T_{ki} transfer function. The transfer function exhibits a very low gain at dc. Therefore, a control circuit, which can achieve a phase margin of $PM = 60°$, an improved bandwidth, and a high gain at dc (> 50 dB) must be designed. A type-II controller, which satisfies the desired properties was selected for this design. The desired crossover frequency was selected as $f_c = 30$ kHz. The type-II controller transfer function in pole-zero form is

$$T_{ci} = T_{cio} \frac{1 + \frac{s}{\omega_{zci}}}{s\left(1 + \frac{s}{\omega_{pci}}\right)}, \tag{3.12}$$

where T_{cio} is the approximate gain at dc, $f_{zci} = \omega_{zci}/2\pi$ is the zero frequency, and $f_{pci} = \omega_{pci}/2\pi$ is the pole frequency [35]. The magnitude and phase plots of the controller transfer function is shown in Fig. 2.24. A phase boost is provided around the crossover frequency f_c and the dc gain requirement was also satisfied. Based on the design provided in [34], [35], the following components were selected for the controller: $R_1 = 1$ kΩ, $R_2 = 1.1$ kΩ, $C_1 = 50$ nF, and $C_2 = 1$ nF. The inner-current loop gain is, therefore,

$$T_i = \frac{v_{ei}}{v_{fi}} = T_{ci} T_m T_{pi} R_s T_f. \tag{3.13}$$

Fig. 2.27 in Chapter 2 shows the loop gain relevant to the inner-current loop. The phase margin was $PM = 60°$ and the gain margin was $GM = -21$ dB.

With the closed-inner loop designed, the true-average buck-boost mode controlled dc-dc converter was built and tested to validate the steady-state characteristics. The dc reference voltage was set at $V_{RI} = V_{Rs} = 1.87$ V. Wide-bandwidth operational

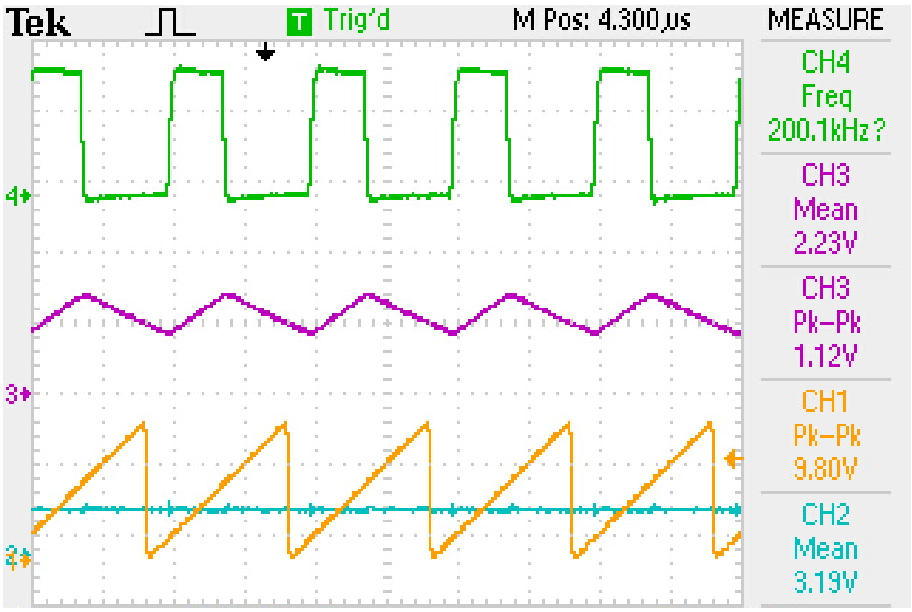

Figure 3.40: Steady-state waveforms: (a) Gate-to-source voltage (*top*), (b) inductor current (*middle*), and (c) sawtooth waveform and control voltage (*bottom*).

amplifiers LT1630 by Linear Technologies was used in the pulse-width modulator and current-loop controller stages. The gate-driver IR2117 was used to produce the required gate-to-source voltage waveform for the switch S. Fig. 3.40 shows the waveforms of the gate-to-source voltage v_{GS}, inductor current i_L, control voltage v_{CI}, and the sawtooth voltage v_{saw}. The following values were measured for the waveforms shown in Fig. 3.40: duty cycle $D = 0.372$, inductor current ripple $\Delta i_L = 0.9$ A, average inductor current $I_L = 2.23$ A, and average control voltage $V_{CI} = 3.19$ V. The measured ripple in the sensed voltage and the feedback voltage were $\Delta V_{Rs} = 0.63$ V and $\Delta V_{FI} = 0.25$ V to give $\Delta V_{FI}/\Delta V_{Rs} \approx 0.4$. The measured output voltage was $V_O = -5$ V.

3.7 Reference Voltage-to-Inductor Current Transfer Function T_{icl}

From Chapter refchap:Chapter05, the closed-loop reference voltage-to-inductor current transfer function is

$$T_{icl}(s) = \left.\frac{i_l(s)}{v_{ri}(s)}\right|_{v_i=i_o=0} = \frac{T_{ci}T_mT_{pi}}{1+T_{ci}T_mT_{pi}T_fR_s} = \frac{T_{ci}T_mT_{pi}}{1+T_i}. \tag{3.14}$$

Fig. 3.41 compares the theoretical and experimental magnitude and phase plots of the T_{icl} transfer function. The experimental prototype of the closed-loop buck-boost converter was built including the controller circuit. An HP4194A gain-phase analyzer was used to obtain the Bode plots for the described transfer functions. Pearson 411 wide-bandwidth current transformer with a gain 0.1 A/V = −20 dB was used to record the inductor current. DC blocking capacitors of value $C_B = 47\ \mu$F with negligible series resistances were used at the small-signal voltage injection and extraction nodes. The current-probe compensation of −20 dB was added to T_{icl}. The frequency response of the current injection transformer was taken into account to obtain the final measurement data. A propagation delay in the logic gates in the gate-driver and pulse-width modulator was taken into account as it affected the phase of T_{pi} at high frequencies [21]. The delay was modeled using the first-order Padé approximation and is expressed in Laplace domain as

$$e^{-sT_d} \approx \frac{1-s\frac{T_d}{2}}{1+s\frac{T_d}{2}} = -\frac{s-\frac{2}{T_d}}{s+\frac{2}{T_d}} \tag{3.15}$$

and the transfer function was multiplied with the power stage transfer function T_{pi}. Therefore, the modified reference-to-inductor current transfer function is

$$T_{icl}(s) = \frac{T_{ci}T_mT_{pi}e^{-sT_d}}{1+T_ie^{-sT_d}}. \tag{3.16}$$

With the inclusion of the inner-current loop, the control bandwidth was improved from 10 kHz to 30 kHz. The gain at dc was $T_{icl}(0)$ = 3.71 dB = 1.53 A/V. The

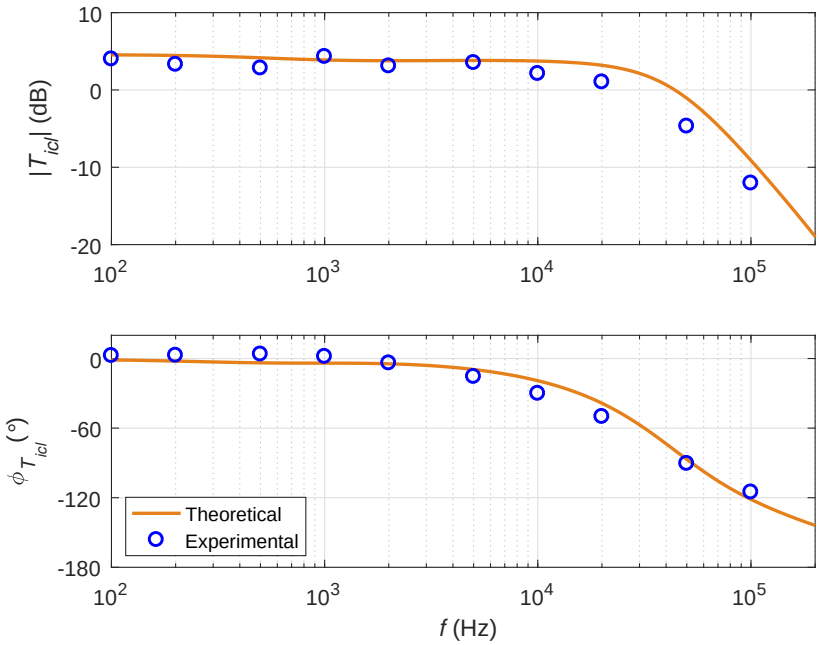

Figure 3.41: Experimental validation of theoretically predicted reference voltage-to-inductor current transfer function T_{icl}.

inductor current response for a step change in the reference voltage was plotted on MATLAB using the transfer function given in (3.16) as shown in Fig. 3.42. For a step change in the reference voltage by $\Delta V_{RI} = 1$ V, the inductor current changes by $\Delta I_L = T_{icl}(0) \times 1 = 1.53 \times 1 = 1.53$ A. The theoretically obtained inductor current response was validated experimentally as shown in Fig. 3.43. For a step change in reference voltage by $\Delta V_{RI} = 1$ V, the inductor current increased by $\Delta I_L = 1.69$ A from the steady-state value $I_L = 2.17$ A to $I_L = 3.86$ A to give $T_{icl}(0) = \Delta I_L / \Delta V_{RI} = 1.69$ A/V. A good agreement between theory and measurements can be observed.

3.8 Reference Voltage-to-Duty Cycle Transfer Function T_{di}

The critical path from the reference voltage to the output voltage is controlled by the duty cycle as represented in Fig. 2.4(c). The transfer function between v_{ri} and d is

$$T_{di} = \frac{d}{v_{ri}} = \frac{T_{ci} T_m}{1 + T_{ci} T_m T_f R_s T_{pi}}. \tag{3.17}$$

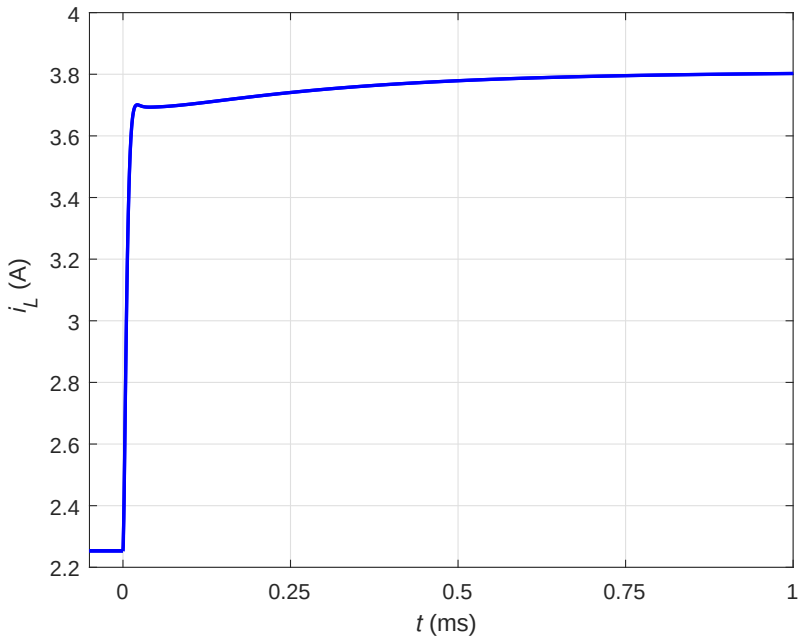

Figure 3.42: Theoretical inductor current response for step change in current-reference voltage by $\Delta V_{RI} = 1$ V.

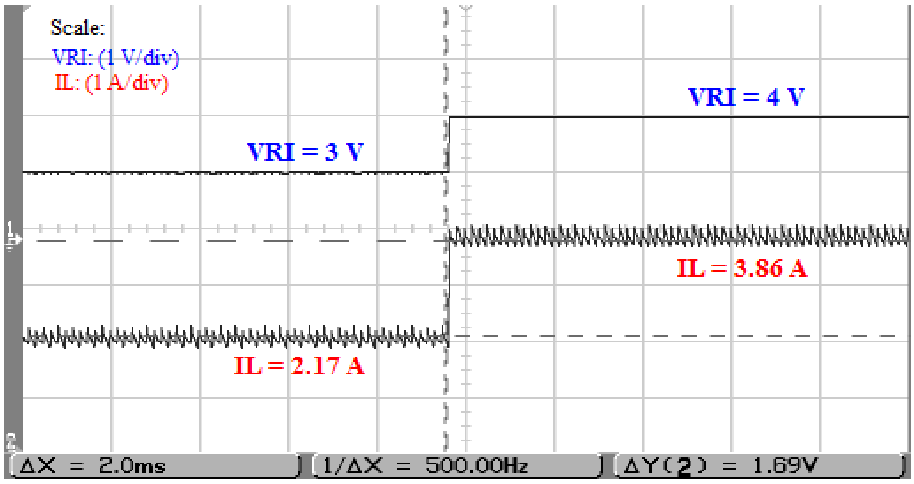

Figure 3.43: Measured inductor current response for step change in current-reference voltage by $\Delta V_{RI} = 1$ V.

The inner-current loop modifies the path between v_{ri} and v_o by providing a phase boost, especially near the region, where the effect of RHP zero is significant. Therefore, in this modeling approach, the power-stage poles and zeros are unaffected and the power-stage transfer function is of order two. The response is improved by incor-

porating the poles and zeros into the inner-current-loop transfer function. This is a non-physical transfer function, and therefore, has not been verified experimentally.

3.9 Reference Voltage-to-Output Voltage Transfer Function T_{picl}

As discussed earlier, the duty cycle governs both the inductor current and the output voltage. Therefore, using Fig. 2.4(c), the closed-loop reference-to-output voltage transfer function is

$$T_{picl}(s) = \left.\frac{v_o(s)}{v_{ri}(s)}\right|_{v_i=i_o=0} = \frac{T_{ci}T_mT_p}{1+T_{ci}T_mT_{pi}T_fR_s} = \frac{T_{ci}T_mT_p}{1+T_i}. \tag{3.18}$$

Fig. 3.44 compares the theoretical and measured magnitude and phase plots of the T_{picl}. The gain at dc is nearly $T_{picl}(0) = 1.52$ dB $= 1.19$ V/V. The phase plots produce a phase shift of 180° due to an inverted output voltage. The RHP zero occurs at $f_{zp} = 32.23$ kHz. For the power-stage transfer function T_p, the RHP zero causes a phase drop at low duty ratios. However, with the introduction of the inner-current-loop, the transfer function T_{di} causes a phase boost in T_{picl}, specifically around f_{zp}. The phase at $f_s/2$ is less than unity and is accomplished by the high-frequency controller pole and the pole of the low-pass filter. Therefore, the small-signal model of the true-average current-mode control shows an improved closed-loop stability and a high phase, especially in the vicinity of the voltage-loop crossover frequency. As a result, the voltage loop can be designed using simpler controllers such as Type-II. Fig. 3.45 shows the theoretically obtained output voltage response for a step increment in current-reference voltage v_{RI} by 1 V. For a 1 V step change in the reference voltage, the output voltage changes by $\Delta V_O = T_{picl}(0) \times 1 = 1.09 \times 1 = 1.09$ V. The measured output voltage response is shown in Fig. 3.46. For a step change in reference voltage by $\Delta V_{RI} = 0.87$ V, v_O increased by $\Delta V_O = 0.99$ V from the steady-state value $V_O = -5$ V to $V_O = -5.99$ V to give $T_{picl}(0) = \Delta V_O/\Delta V_{RI} = 1.14$. Hence, a good

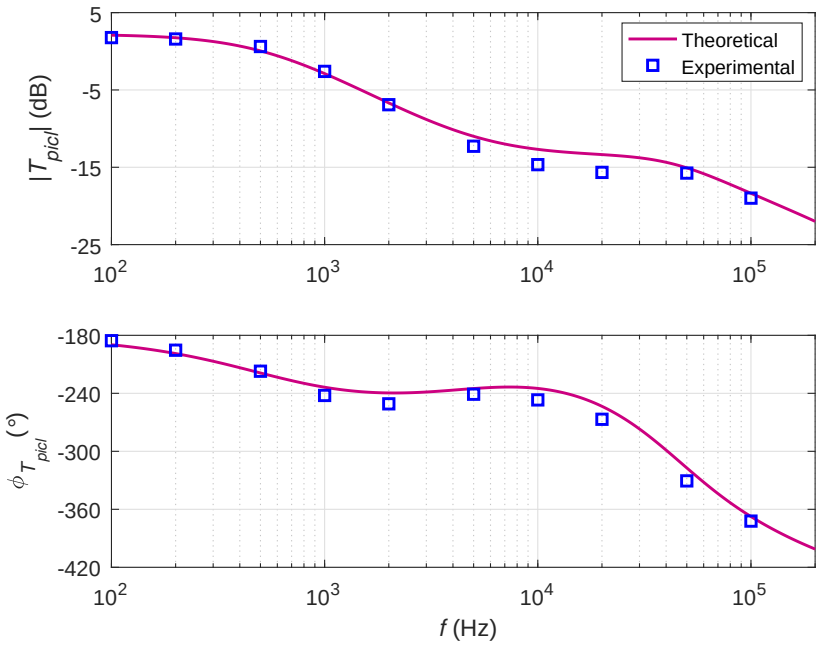

Figure 3.44: Experimental validation of theoretically obtained reference voltage-to-output voltage transfer function T_{picl}.

agreement between model prediction and measurements was observed.

Fig. 3.47 shows the experimentally obtained Bode magnitude and phase plots of the closed-loop input voltage-to-inductor current transfer function. This is a disturbance path transfer function. It can be seen that a large attenuation factor is offered to the disturbance in the input voltage by the inner current loop as compared to the open loop. The measured results shows good agreement with the theoretically predicted results.

Fig. 3.48 shows the experimentally obtained Bode magnitude and phase plots of the closed-loop input voltage-to-output transfer function. This is a disturbance path transfer function. The output voltage attenuation offered by the current loop for a disturbance in the input voltage is not very strong. However, the attenuation can be further improved by incorporating the outer voltage loop. The measured results shows good agreement with the theoretically predicted results.

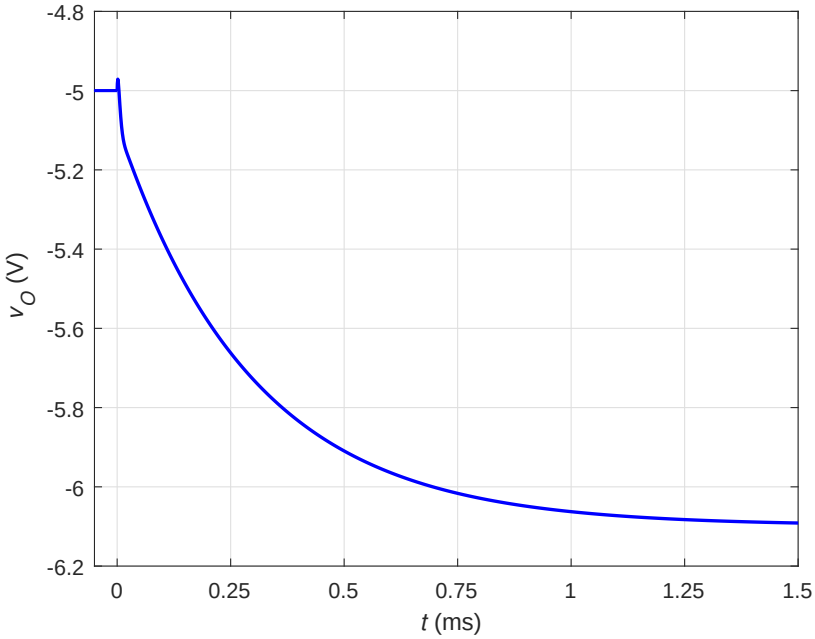

Figure 3.45: Theoretical output voltage response for step change in current-reference voltage by $\Delta V_{RI} = 1$ V.

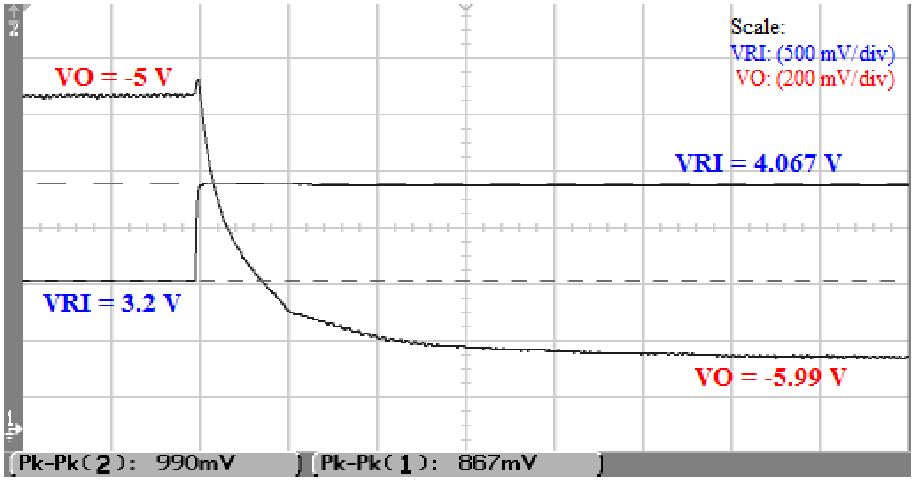

Figure 3.46: Measured output voltage response for step change in current-reference voltage by $\Delta V_{RI} = 0.87$ V.

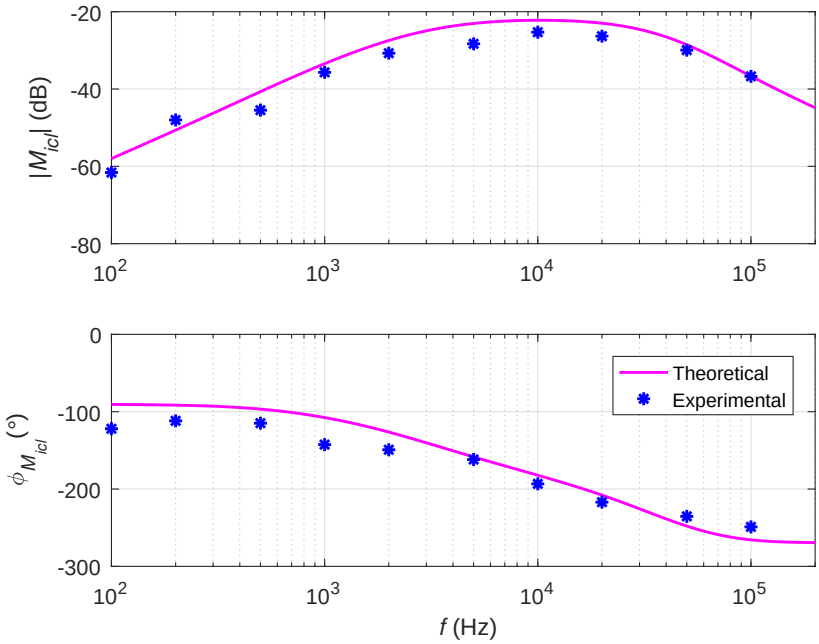

Figure 3.47: Experimental validation of theoretically obtained input voltage-to-inductor current transfer function M_{icl}.

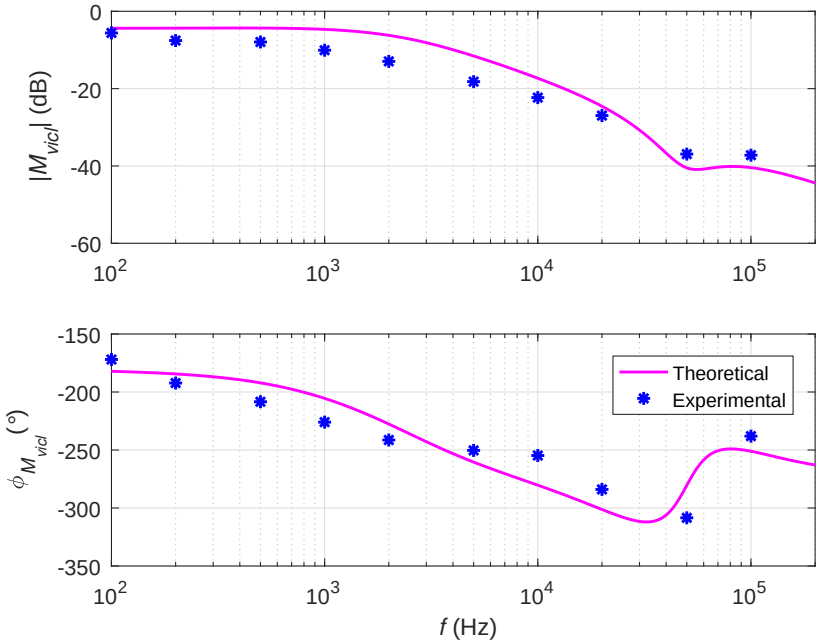

Figure 3.48: Experimental validation of theoretically obtained input voltage-to-output voltage transfer function M_{vicl}.

4 True-Average Current-Mode Control of Boost DC-DC Converter

The circuit of a pulse-width modulated PWM boost converter is shown in Fig. 4.1. The circuit consists of a power MOSFET S, a diode D_o, an inductor L, a filter capacitor C, and a load resistor R_L. The switch is turned ON and OFF at a switching frequency f_s and at a duty cycle D. The parasitic resistances of the passive and semiconductor components are considered in the analysis. The equivalent series resistances of the inductor and capacitor are r_L and r_C, respectively. The ON-state resistance of the MOSFET and the ON-resistance of the diode are r_{DS} and R_F, respectively, and the diode forward voltage is V_F. The dc voltage transfer function of the ideal boost converter in CCM is

$$M_{VDC(lossless)} = \frac{V_O}{V_I} = \frac{1}{1-D} \tag{4.1}$$

to produce the duty cycle for the loss-less boost converter as

$$D = 1 - \frac{V_I}{V_O}. \tag{4.2}$$

The aims of this chapter are:

1. To describe dc characteristics.
2. To introduce small-signal linear model.
3. To derive and analyze the open-loop power stage transfer functions.
4. To derive and analyze the open-loop input and output impedances.
5. To design and analyze a compensator circuit.
6. To derive and analyze the closed inner-current-loop transfer functions.

4.1 DC Characteristics

Fig. 4.2 shows the the idealized current and voltage waveforms of the switching network of the boost converter. The small-ripple approximation is made, where the amplitude of the inductor current ripple due to the switching action is considered to be much lower than the dc component of the inductor current. As a result, the peak value of the switch current is equal to the average value of the inductor current I_L. The average component of the switch current is, therefore

$$I_S = \frac{1}{T}\int_0^T i_s dt = \frac{1}{DT}\int_0^T I_L dt = DI_L. \tag{4.3}$$

Notice that the average switch current is a function of the average inductor current and the duty cycle. By the principle of circuit-averaging, the switch can be replaced by a current source dependent on the inductor current and the duty cycle. Similarly approach can be adopted to model the diode. The average diode voltage is

$$V_D = \frac{1}{T}\int_0^T v_d dt = \frac{1}{DT}\int_0^T (V_O) dt = DV_O. \tag{4.4}$$

The diode can be replaced by a voltage source dependent on the duty cycle and the output voltage. Since the voltage across the diode is negative, when the switch is ON, the negative sign can be incorporated into the model by reversing the polarities of the controlled voltage source. The switch and diode are first replaced by their equivalent current-controlled current source the voltage-controlled voltage source, respectively. At dc, the capacitor is an open-circuit and the inductor is a short-circuit. Such

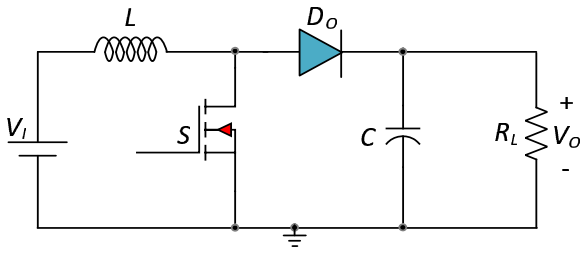

Figure 4.1: DC model of the PWM boost converter.

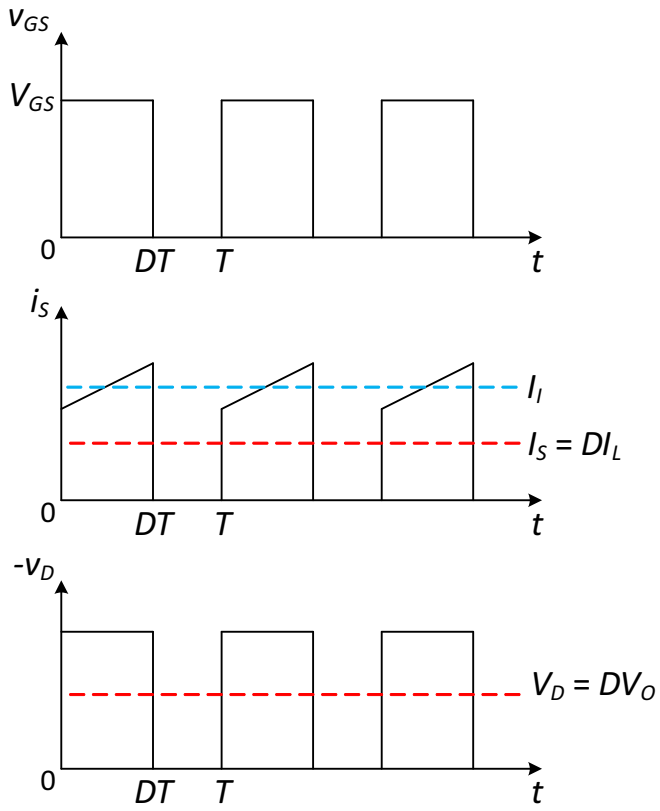

Figure 4.2: Waveforms of ideal switching network. (a) gate-to-source voltage of switch (b) switch current, and (c) diode voltage.

substitutions result in the dc, averaged model of the boost converter as shown in Fig. 4.3. This form of circuit modeling presents another advantage, where the component parasitic resistances can be lumped and placed in the inductor branch. The equivalent averaged resistance placed in the inductor branch is

$$r = Dr_{DS} + (1 - D)R_F + r_L. \tag{4.5}$$

The steady-state performance of the converter can be analyzed using the dc model. Applying KCL at the node connecting the inductor, switch, and diode results in

$$I_L = DI_L + I_O. \tag{4.6}$$

The dc input current I_I and the average inductor current I_L are equal. The dc current transfer function is therefore,

$$M_{IDC} = \frac{I_O}{I_L} = 1 - D. \tag{4.7}$$

Applying KVL to the loop between the supply voltage and the load

$$V_I = rI_L - DV_O + V_O = r\frac{I_O}{1-D} + V_O(1-D) = r\frac{V_O}{R_L(1-D)} + V_O(1-D), \tag{4.8}$$

to yield the dc voltage transfer function of the lossy boost dc-dc converter as

$$\begin{aligned} M_{VDC(lossy)} = \frac{V_O}{V_I} &= \frac{1}{\frac{r}{R_L(1-D)} + (1-D)} = \frac{1}{(1-D)\left[1 + \frac{r}{R_L(1-D)^2}\right]} \\ &= \eta M_{VDC(lossless)}, \end{aligned} \tag{4.9}$$

where the converter efficiency excluding the switching loss and the loss in the filter capacitor is

$$\eta = \frac{P_O}{P_I} = \frac{1}{1 + \frac{r}{R_L(1-D)^2}} = \frac{1}{1 + \frac{Dr_{DS} + (1-D)R_F + r_L}{R_L(1-D)^2}}. \tag{4.10}$$

Therefore, the duty cycle of a lossy boost dc-dc converter is

$$D = 1 - \frac{\eta}{M_{VDC(lossless)}}. \tag{4.11}$$

4.2 Small-Signal Model of PWM Boost converter for CCM

The dc model is perturbed about the steady-state operating point resulting in large-signal nonlinear model. The large-signal quantities can be expressed as the sum of dc and ac components as

$$i_S = I_S + i_s. \tag{4.12}$$

$$i_L = I_L + i_l. \tag{4.13}$$

$$v_D = V_D + v_d. \tag{4.14}$$

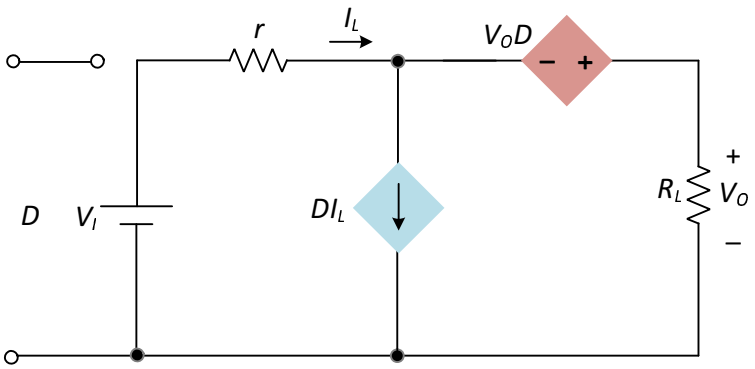

Figure 4.3: DC and low-frequency model of pulse-width modulated boost dc-dc converter.

$$v_I = V_I + v_i. \tag{4.15}$$

$$v_O = V_O + v_o. \tag{4.16}$$

$$d_T = D + d. \tag{4.17}$$

Hence, from (4.3) and (4.4)

$$i_S = d_T i_L = (D + d)(I_L + i_l) \tag{4.18}$$

and

$$v_D = d_T v_O = (D + d)(V_O + v_o). \tag{4.19}$$

In (4.18) and (4.19), the high-order ac terms are eliminated by using the small signality conditions yielding a linearized large signal model. The dc and ac terms are separated to obtained dc averaged model as shown in Fig. 4.3 and the linear, averaged small-signal model as shown in Fig. 4.4.

4.3 Design Example

The subsequent analysis is done on the boost converter designed for the following specifications.

1. Supply voltage $V_I = 12$ V.

2. Output voltage $V_O = 20$ V.

3. Output power $P_O = 10$ W.

4. Load resistance $R_L = 40\ \Omega$.

5. Switching frequency $f_s = 100$ kHz.

6. The inductance to ensure CCM operation $L = 50\ \mu$H.

7. The filter capacitance $C = 100\ \mu$F.

The equivalent series resistances of the inductor is $r_L = 30\ \text{m}\Omega$ and the capacitor is $r_C = 25\ \text{m}\Omega$. The selected MOSFET was IRF540 by International Rectifiers and the selected diode was MBR10100 by Vishay Semiconductors. From their respective datasheets, the ON-state resistance of the MOSFET and the on-resistance of the diode were $r_{DS} = 0.11\ \Omega$ and $R_F = 0.07\ \Omega$. Diode forward voltage is $V_F = 0.3$ V. The calculated value of converter efficiency is $\eta = 99\%$. The equivalent averaged resistance $r \approx 0.1162\ \Omega$. The open-loop dc quantities from Section 4.1 are given in Table 4.1.

Table 4.1: Summary of calculated values for dc quantities

Variable	**Value**
I_I	0.8333 A
I_O	0.5 A
M_{IDC}	0.6
M_{VDC}	1.6667
I_L	0.8333 A
D	0.4048

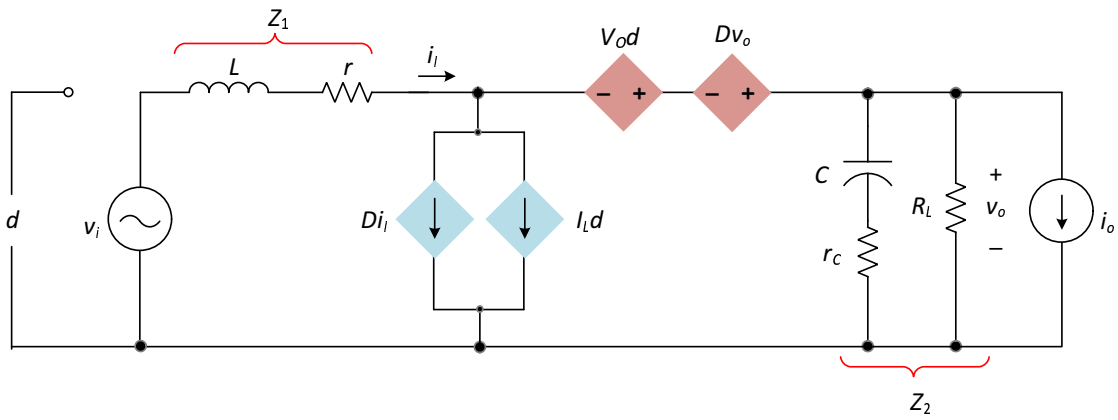

Figure 4.4: Small-signal model of the pulse-width-modulated boost dc-dc converter in continuous-conduction-mode (CCM).

4.4 Power Stage Transfer Functions

The following power stage transfer functions are discussed in the subsequent section.

1. Duty cycle-to-output voltage transfer function T_p (Control).

2. Duty cycle-to-inductor current transfer function T_{pi} (Control).

3. Input voltage-to-output voltage transfer function M_v (Disturbance).

4. Input voltage-to-inductor current transfer function M_{vi} (Disturbance).

5. Reverse current gain A_i (Disturbance).

6. Input impedance Z_i (Disturbance).

7. Output impedance Z_o (Disturbance).

The small-signal model of the PWM boost converter is shown in Fig. 4.4. The current through the parallel combination of the load resistor and the filter capacitor is

$$i_{Z2} = \frac{v_o}{Z_2}. \tag{4.20}$$

The current through the inductor is

$$i_l = Di_l + I_L d + \frac{v_o}{Z_2}. \tag{4.21}$$

The input current is

$$i_i = i_l. \tag{4.22}$$

Applying Kirchhoff's voltage law, the output voltage is

$$v_o = v_i - i_l Z_1 + Dv_o + V_o d. \tag{4.23}$$

The impedances Z_1 and Z_2 are

$$Z_1 = r + sL \tag{4.24}$$

and

$$Z_2 = R_L || \left(r_c + \frac{1}{sC} \right) = \frac{R_L \left(r_C + \frac{1}{sC} \right)}{R_L + r_C + \frac{1}{sC}}. \tag{4.25}$$

4.4.1 Duty Cycle-to-Output Voltage Transfer Function T_p

The duty cycle-to-output voltage transfer function is obtained by setting $v_i = 0$ and $i_o = 0$ in Fig. 4.4. The control-to-output transfer function in the impedance form is

$$T_p(s) = \left. \frac{v_o(s)}{d(s)} \right|_{v_i = i_o = 0} = \frac{V_O}{1 - D} \frac{1 - \frac{Z_1}{(1-D)^2 R_L}}{1 + \frac{Z_1}{(1-D)^2 Z_2}} \tag{4.26}$$

Substituting (4.24) and (4.25) in (4.26) gives the control-to-output transfer function in s-domain as

$$T_p(s) = \left. \frac{v_o(s)}{d(s)} \right|_{v_i = i_o = 0} = T_{px} \frac{(s + \omega_{zn})(s - \omega_{zp})}{s^2 + 2\xi\omega_0 s + \omega_0^2} = T_{po} \frac{\left(1 + \frac{s}{\omega_{zn}} \right) \left(1 - \frac{s}{\omega_{zp}} \right)}{\left(\frac{s}{\omega_0} \right)^2 + \frac{2\xi s}{\omega_0} + 1}, \tag{4.27}$$

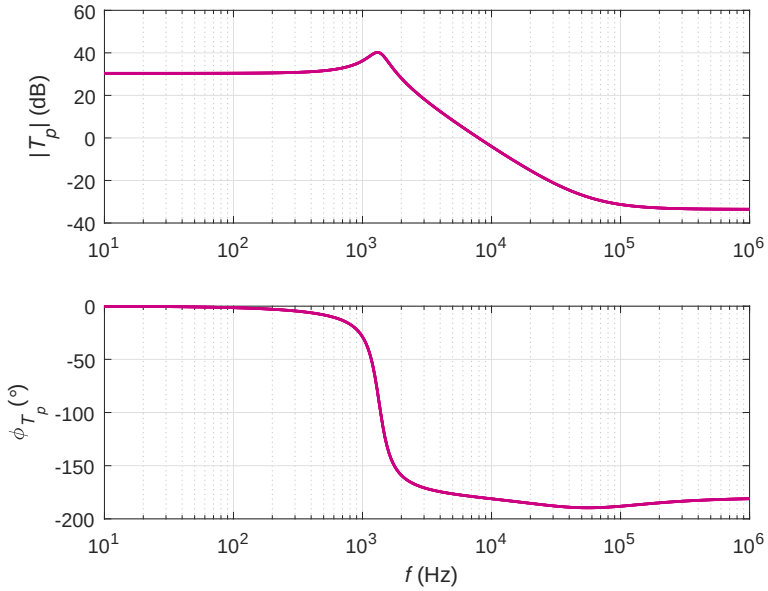

Figure 4.5: Theoretically obtained magnitude and phase plots of the duty cycle-to-output voltage transfer function T_p.

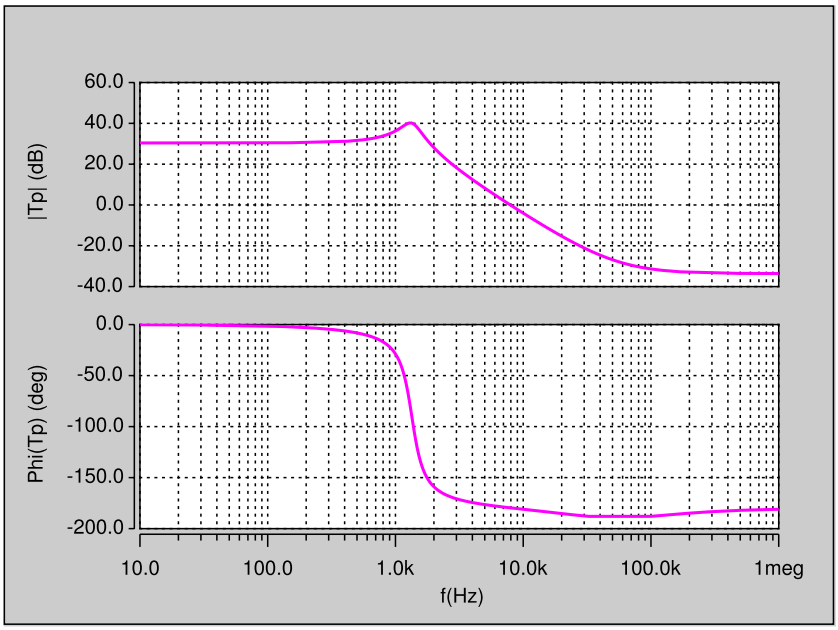

Figure 4.6: Magnitude and phase plots of the duty cycle-to-output voltage transfer function T_p obtained by circuit simulations.

where the dc gain T_{po} is

$$T_{po} = \frac{V_O}{1-D}\frac{R_L(1-D)^2 - r}{R_L(1-D)^2 + r}, \tag{4.28}$$

the gain T_{px} is

$$T_{px} = -\frac{V_O}{1-D}\frac{r_C}{R_L + r_C}, \tag{4.29}$$

the angular corner frequency or the angular undamped natural frequency is

$$\omega_0 = \sqrt{\frac{(1-D)^2 R_L + r}{LC(R_L + r_C)}}, \tag{4.30}$$

the damping ratio is

$$\xi = \frac{L + C[r(R_L + r_C) + (1-D)^2 R_L r_C]}{2\sqrt{LC(R_L + r_C)[(1-D)^2 R_L + r)}}. \tag{4.31}$$

The angular frequency of the left-half plane zero is

$$\omega_{zn} = \frac{1}{r_C C} \tag{4.32}$$

and the angular frequency of the right-half plane zero is

$$\omega_{zp} = \frac{R_L(1-D)^2 - r}{L}. \tag{4.33}$$

Fig. 4.5 shows the theoretically obtained magnitude and phase plots of duty-cycle-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 4.6 shows the magnitude and phase plots of duty-cycle-to-output voltage transfer function using SABER Simulator. The gain at dc and low-frequencies is nearly $T_{p0} = 30.4$ dB $= 33.113$ V/V. The natural corner frequency of the second-order low-pass filter formed by the inductor, capacitor, and load resistor is $f_o =$ 1.35 kHz.

4.4.2 Duty Cycle-to-Inductor Current Transfer Function T_{pi}

The duty cycle-to-output voltage transfer function is obtained by setting $v_i = 0$ and $i_o = 0$ in Fig. 4.4. Setting $v_i = 0$ in (4.21) and rearranging

$$i_l = \frac{V_I d}{Z_1 + Z_2}. \tag{4.34}$$

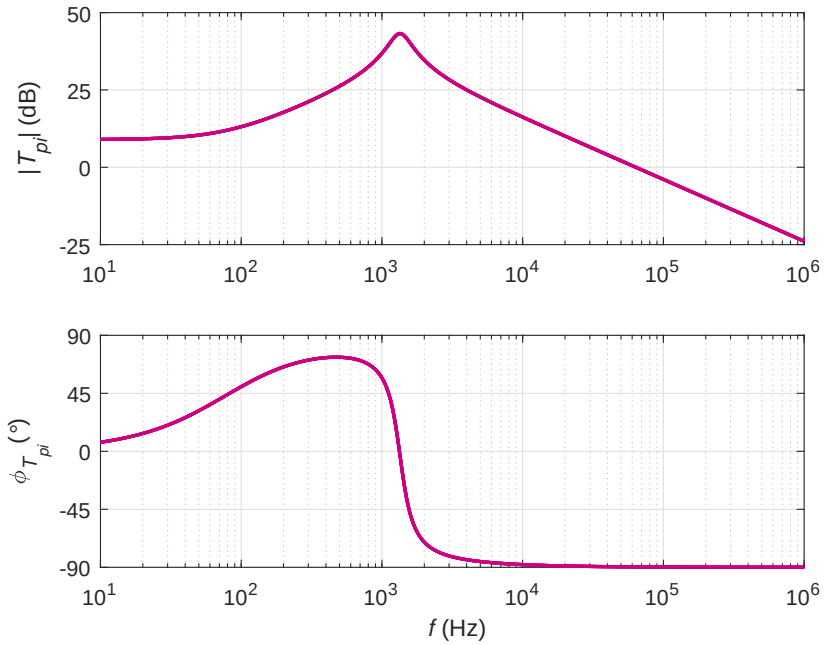

Figure 4.7: Theoretically obtained magnitude and phase plots of the duty cycle-to-inductor current transfer function T_{pi}.

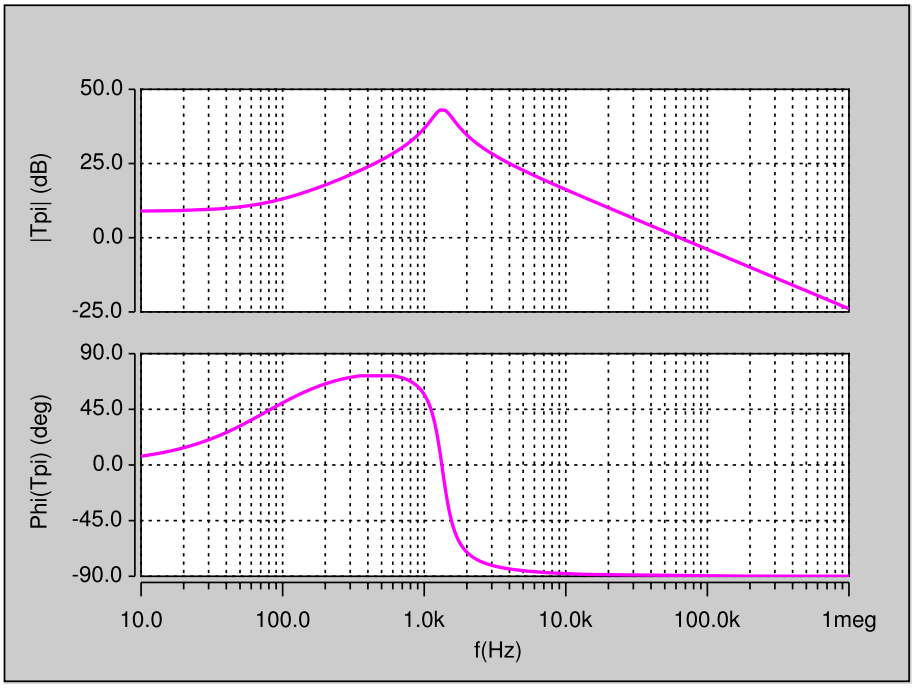

Figure 4.8: Magnitude and phase plots of the duty cycle-to-inductor current transfer function T_{pi} obtained by circuit simulation.

Hence, the control-to-inductor current transfer function is

$$T_{pi}(s) = \left.\frac{i_l(s)}{d(s)}\right|_{v_i=i_o=0} = \frac{V_I}{Z_1 + Z_2}. \tag{4.35}$$

Substituting (4.24) and (4.25) in (4.35) gives the control-to-inductor current transfer function in s-domain as

$$T_{pi}(s) = \left.\frac{i_l(s)}{d(s)}\right|_{v_i=i_o=0} = T_{pix}\frac{(s+\omega_{zi})}{s^2 + 2\xi\omega_0 s + \omega_0^2} = T_{pio}\frac{\left(1 + \dfrac{s}{\omega_{zi}}\right)}{\left(\dfrac{s}{\omega_0}\right)^2 + \dfrac{2\xi s}{\omega_0} + 1}, \tag{4.36}$$

where the dc gain T_{pio} is

$$T_{pio} = \frac{2V_O}{(1-D)^2 R_L + r}, \tag{4.37}$$

the gain T_{pix} is

$$T_{pix} = \frac{V_O(R_L + 2r_C)}{L(R_L + r_C)}, \tag{4.38}$$

and the angular frequency of the left-half plane zero is

$$\omega_{zi} = \frac{1}{C\left(\dfrac{R_L}{2} + r_C\right)}. \tag{4.39}$$

Fig. 4.7 shows the theoretically obtained magnitude and phase plots of duty cycle-to-inductor current transfer function. The theoretical results were validated by simulation. Fig. 4.8 shows the magnitude and phase plots of duty cycle-to-inductor current transfer function using SABER Simulator. The gain at dc and low-frequencies is nearly $T_{pi0} = 8.94$ dB $= 2.8$ V/V. The natural corner frequency of the second-order low-pass filter formed by the inductor, capacitor, and load resistor is $f_o = 1.35$ kHz. The frequency of the left-half plane zero is $f_{zi} = 80$. The gain decreases at the rate of 20 dB/dec beyond f_o. The duty cycle-to-inductor current transfer function for the boost converter exhibits a low-frequency zero f_{zi} and a complex conjugate pole-pair at f_o. The phase starts at zero and rises to 45° due to f_{zi}. This means that at low frequencies, the duty cycle signal leads the inductor current by a particular

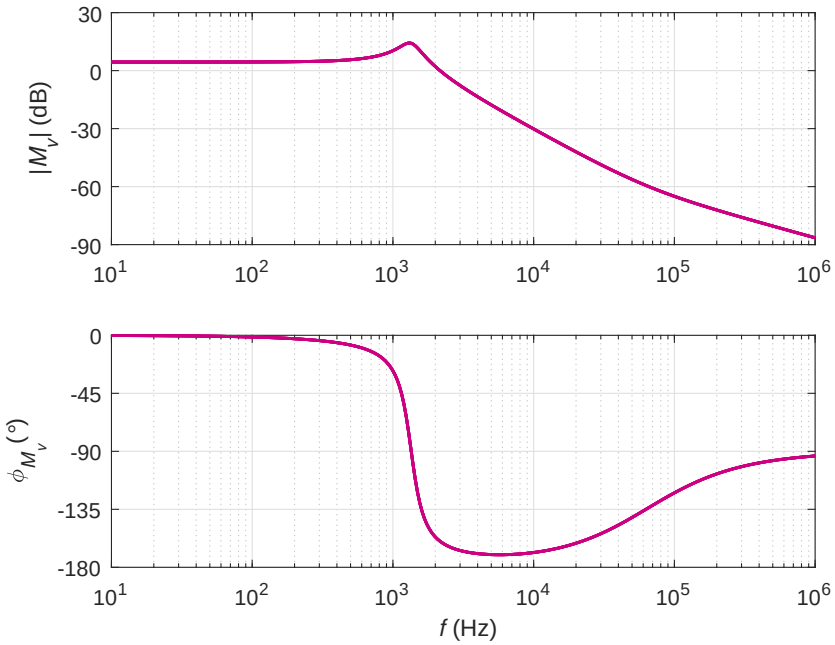

Figure 4.9: Theoretically obtained magnitude and phase plots of the input voltage-to-output voltage transfer function M_v.

phase angle. The bandwidth of T_{pi} is larger than that of T_p. Therefore, the inner current loop presents a faster response in inductor current for change in duty cycle. The low-frequency zero f_{zi} depends on the load resistance R_L and the parameters of the filter capacitance, namely C and r_C. As the value of R_L is decreased at a fixed C, f_{zi} moves towards f_o. The nature of the roots of the characteristic equation (denominator of T_{pi}) or the poles of T_{pi} converts from complex conjugate to real. At a specific minimum load resistance, $f_{zi} \approx f_o$, i.e., f_{zi} cancels the effect of one of the complex conjugate poles at f_o producing a first-order dominant pole system. The dominant pole is therefore caused by the inductor and load resistance. This effect was observed in buck-boost converter as well.

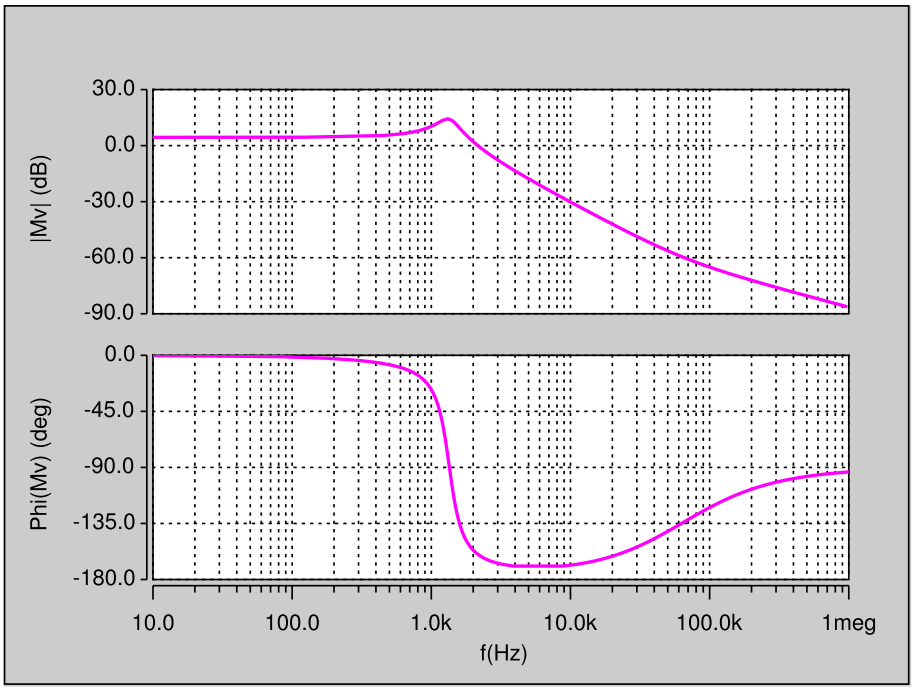

Figure 4.10: Magnitude and phase plots of the input voltage-to-output voltage transfer function M_v obtained by circuit simulation.

4.4.3 Input Voltage-to-Output Voltage Transfer Function M_v

The input voltage-to-output voltage transfer function is obtained by setting $d = 0$ and $i_o = 0$ in Fig. 4.4. The input voltage-to-output voltage transfer function M_v

$$M_v(s) = \left.\frac{v_o(s)}{v_i(s)}\right|_{d=i_o=0} = \frac{Z_2(1-D)}{Z_2(1-D)^2 + Z_1}. \tag{4.40}$$

Substituting (4.24) and (4.25) in (4.35) gives the input voltage-to-output voltage transfer function in s-domain as

$$M_v(s) = \left.\frac{v_o(s)}{v_i(s)}\right|_{d=i_o=0} = M_{vx}\frac{(s+\omega_{zn})}{s^2 + 2\xi\omega_0 s + \omega_0^2} = M_{vo}\frac{\left(1+\dfrac{s}{\omega_{zn}}\right)}{\left(\dfrac{s}{\omega_0}\right)^2 + \dfrac{2\xi s}{\omega_0} + 1}, \tag{4.41}$$

where the dc gain M_{vo} is

$$M_{vo} = \frac{(1-D)R_L}{(1-D)^2 R_L + r} \tag{4.42}$$

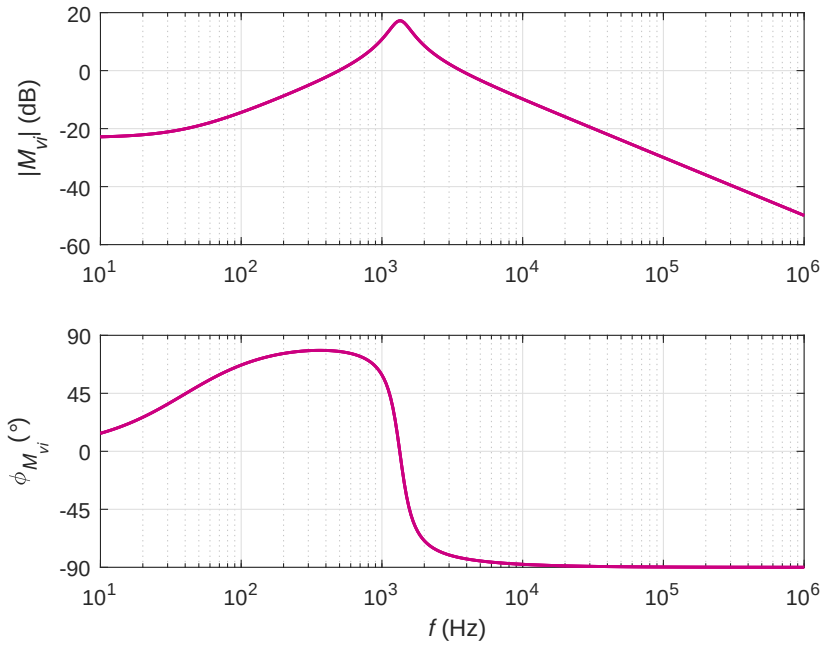

Figure 4.11: Theoretically obtained magnitude and phase plots of input voltage-to-inductor current transfer function M_{vi}.

and the gain M_{vx} is

$$M_{vx} = \frac{(1-D)R_L r_C}{L(R_L + r_C)}. \tag{4.43}$$

The angular frequency of the left-half plane zero is given in (4.32).

Fig. 4.9 shows the theoretically obtained magnitude and phase plots of input voltage-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 4.10 shows the magnitude and phase plots of input voltage-to-output voltage transfer function using SABER Simulator.

4.4.4 Input Voltage-to-Inductor Current Transfer Function M_{vi}

The input voltage-to-inductor current transfer function is obtained by setting $d = 0$ and $i_o = 0$ in Fig. 4.4. Setting $d = 0$ in (4.21) and rearranging

$$i_l = \frac{Dv_i}{Z_1 + Z_2}. \tag{4.44}$$

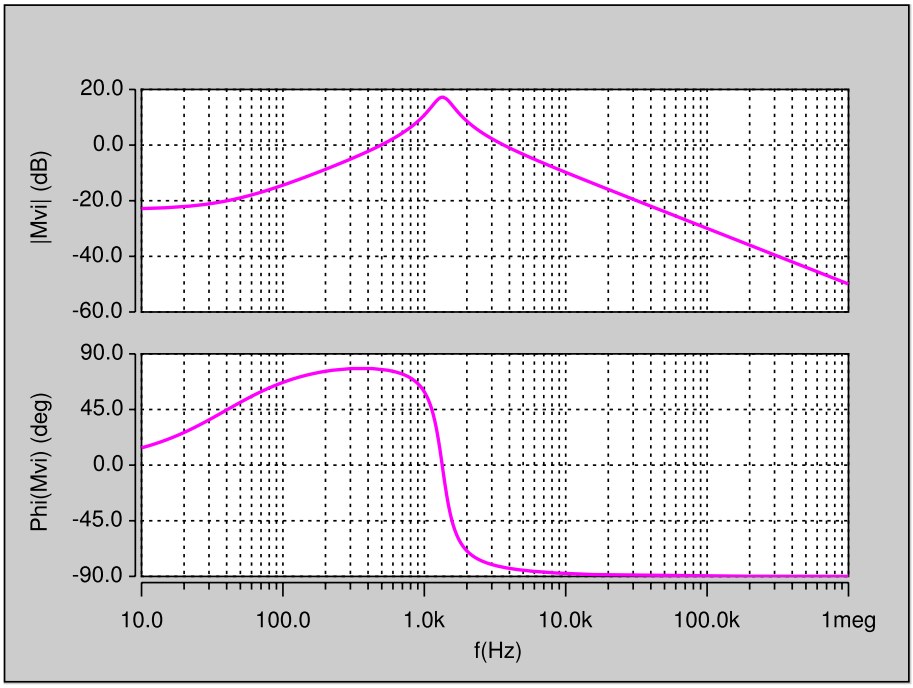

Figure 4.12: Magnitude and phase plots of input voltage-to-inductor current transfer function M_{vi} obtained by circuit simulation.

Hence, the input voltage-to-inductor current transfer function M_{vi} is

$$M_{vi}(s) = \left.\frac{i_l(s)}{v_i(s)}\right|_{d=i_o=0} = \frac{1}{Z_1 + (1-D)^2 Z_2}. \tag{4.45}$$

Substituting (4.24) and (4.25) in (4.45) gives the input voltage-to-inductor current transfer function in s-domain as

$$M_{vi}(s) = \left.\frac{i_l(s)}{v_i(s)}\right|_{d=i_o=0} = M_{vix}\frac{(s+\omega_{zi})}{s^2 + 2\xi\omega_0 s + \omega_0^2} = M_{vio}\frac{\left(1+\dfrac{s}{\omega_{zi}}\right)}{\left(\dfrac{s}{\omega_0}\right)^2 + \dfrac{2\xi s}{\omega_0} + 1}, \tag{4.46}$$

where the dc gain M_{vio} is

$$M_{vio} = \frac{1}{(1-D)^2 R_L + r}, \tag{4.47}$$

the gain M_{vix} is

$$M_{vix} = \frac{1}{L}, \tag{4.48}$$

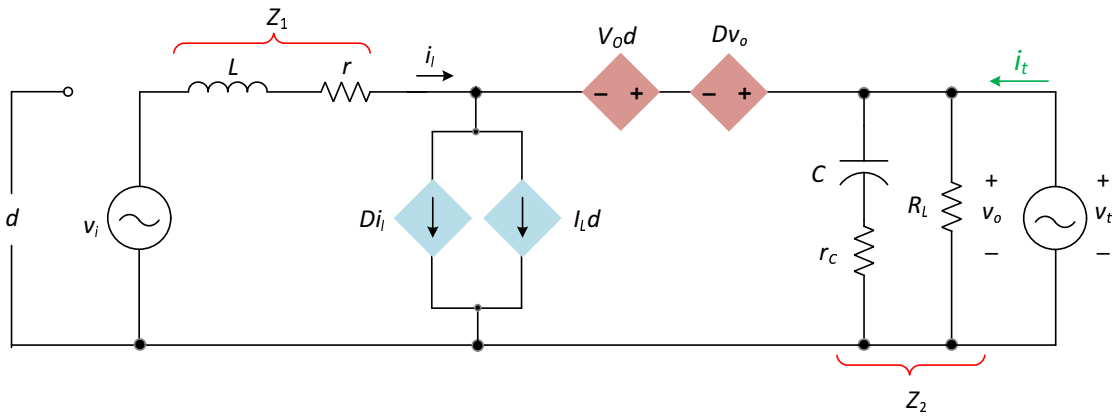

Figure 4.13: Small-signal model of the pulse-width modulated buck dc-dc converter in CCM to derive output current-to-inductor current transfer function A_i.

and the angular frequency of the left-half plane zero is

$$\omega_{zi} = \frac{1}{C(R_L + r_C)}. \tag{4.49}$$

Fig. 4.11 shows the theoretically obtained magnitude and phase plots of input voltage-to-inductor current transfer function. The theoretical results were validated by simulation. Fig. 4.12 shows the magnitude and phase plots of input voltage-to-inductor current transfer function using SABER Simulator. The gain at dc is $M_{vi0} = -23.1$ dB $= 0.07$ V/V. Through the M_{vi} current-loop relevant transfer function, one can observe that the current loop offers a low audio susceptibility at dc than that provided by the voltage-loop transfer function M_v. All the other frequency-domain properties remain identical to T_{pi}.

4.4.5 Reverse Current Gain A_i

The small-signal model to derive output-to-inductor current transfer function is shown in Fig. 4.13. This model is obtain by setting $v_i = 0$ and $d = 0$. An independent voltage source v_t is applied at the output, which forces a current i_t. The output current-to-inductor current transfer function or reverse current transfer function A_i

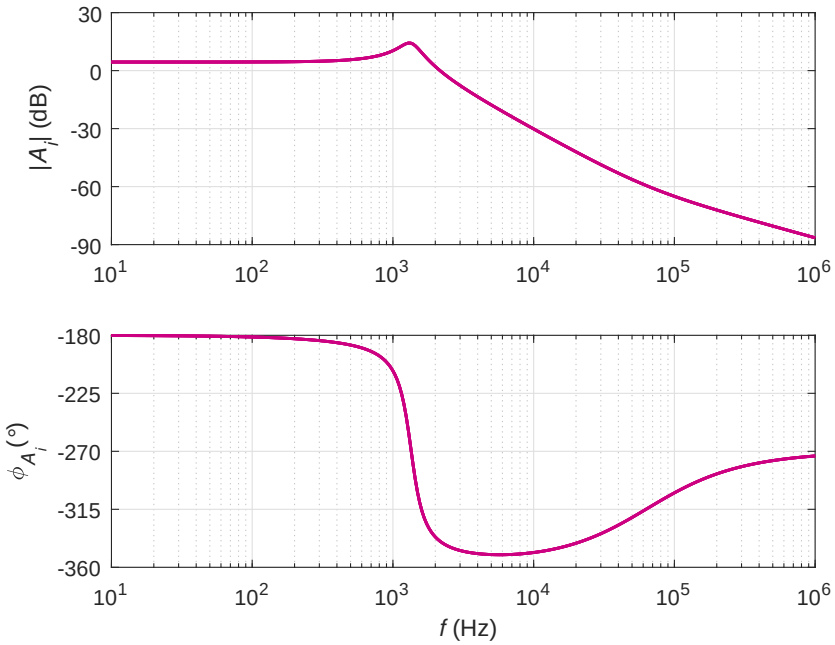

Figure 4.14: Theoretically obtained magnitude and phase plots of the output current-to-inductor current transfer function A_i.

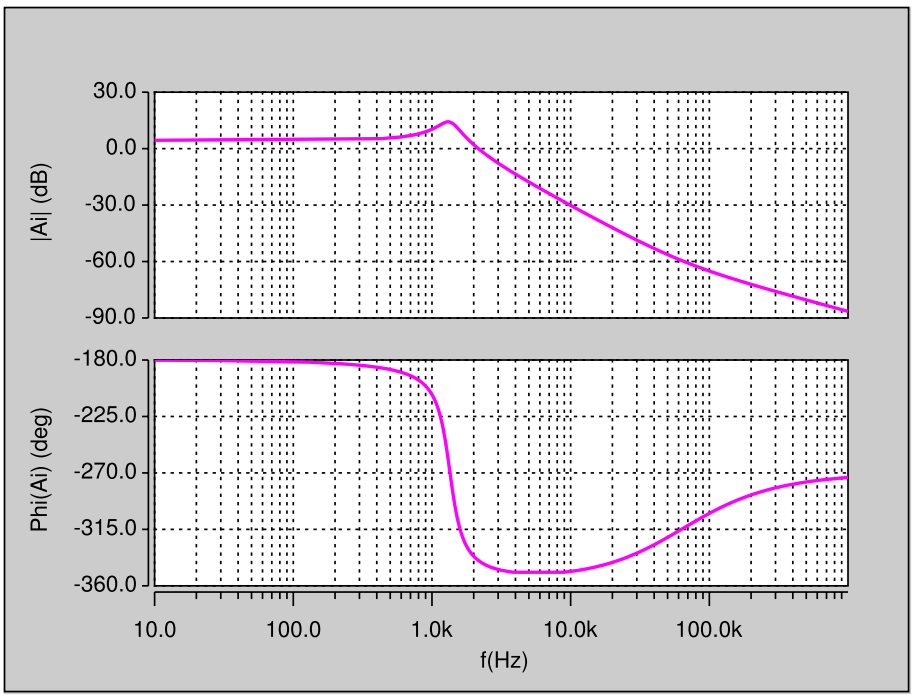

Figure 4.15: Magnitude and phase plots of the output current-to-inductor current transfer function A_i obtained by circuit simulation.

is

$$A_i(s) = \frac{i_l(s)}{i_o(s)}\bigg|_{d=v_i=0} = \frac{(1-D)Z_2}{Z_1 + (1-D)^2 Z_2}. \tag{4.50}$$

Substituting (4.24) and (4.25) in (4.50) gives the output current-to-inductor current transfer function in s-domain as

$$A_i(s) = \frac{i_l(s)}{i_o(s)}\bigg|_{d=v_i=0} = A_{ix}\frac{(s+\omega_z)}{s^2 + 2\xi\omega_0 s + \omega_0^2} = A_{io}\frac{\left(1 + \dfrac{s}{\omega_z}\right)}{\left(\dfrac{s}{\omega_0}\right)^2 + \dfrac{2\xi s}{\omega_0} + 1}, \tag{4.51}$$

where the dc gain A_{io} is

$$A_{io} = \frac{(1-D)R_L}{(1-D)^2 R_L + r}, \tag{4.52}$$

the gain A_{ix} is

$$A_{ix} = \frac{(1-D)R_L r_C}{L(R_L + r_C)}, \tag{4.53}$$

and the angular frequency of the left-half plane zero ω_z is given in (4.32).

Fig. 4.14 shows the theoretically obtained magnitude and phase plots of output-to-inductor current transfer function. The theoretical results were validated by simulation. Fig. 4.15 shows the magnitude and phase plots of output-to-inductor current transfer function using SABER Simulator. The gain at dc is $A_{i0} = 4.45$ dB $= 1.67$ A/A, i.e., the reverse current gain is unity at dc and low-frequencies up to nearly f_o. Beyond f_o the impedance offered by the capacitor branch is lower than the inductor and the small-signal output current begins to flow into the capacitor. Therefore, the gain reduces by -40 dB per decade.

4.4.6 Open-Loop Input Impedance Z_i

The open-loop input impedance is obtained by setting $d = 0$ and $i_o = 0$ in fig. 4.4. The open-loop input impedance is

$$Z_i(s) = \frac{v_i(s)}{i_i(s)}\bigg|_{d=i_o=0} = Z_1 + Z_2(1-D)^2. \tag{4.54}$$

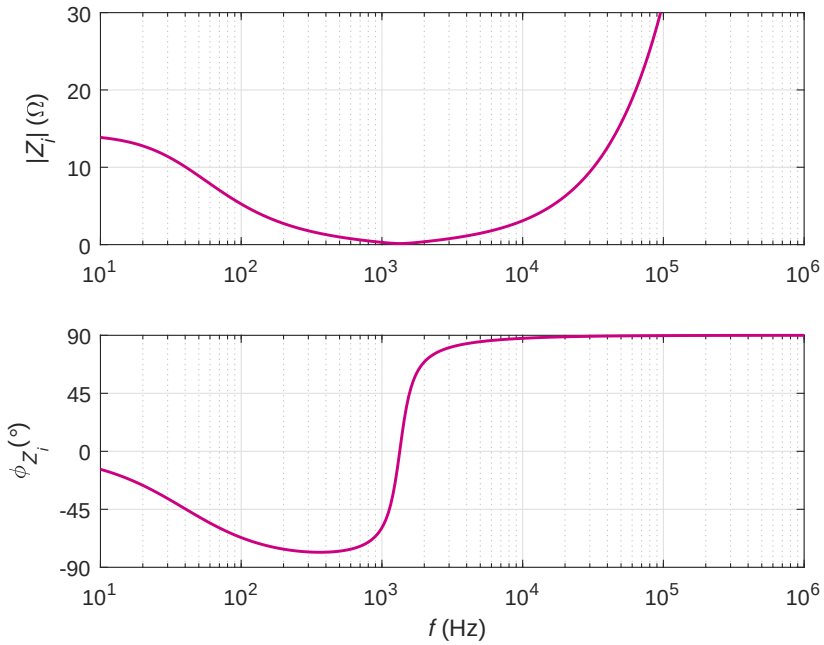

Figure 4.16: Theoretically obtained magnitude and phase plots of the input impedance Z_i.

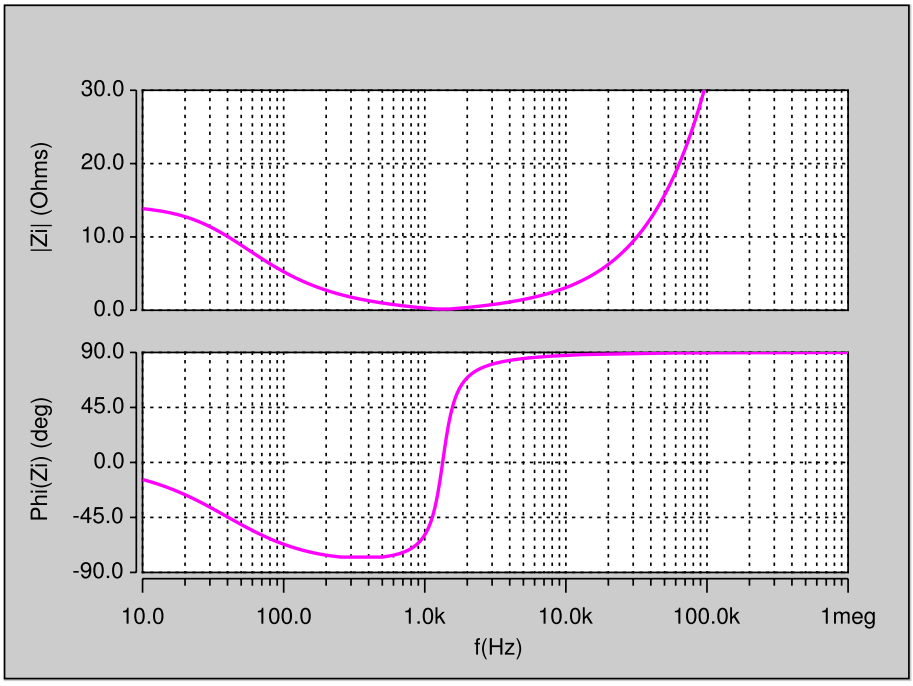

Figure 4.17: Magnitude and phase plots of the input impedance Z_i obtained by circuit simulation.

Substituting (4.24) and (4.25) in (4.54) gives the output current-to-inductor current transfer function in s-domain as

$$Z_i(s) = \left.\frac{v_i(s)}{i_i(s)}\right|_{d=i_o=0} = Z_{ix}\frac{s^2 + 2\xi\omega_0 s + \omega_0^2}{(s+\omega_{zvi})} = Z_{io}\frac{\left(\frac{s}{\omega_0}\right)^2 + \frac{2\xi s}{\omega_0} + 1}{\left(1 + \frac{s}{\omega_{zvi}}\right)}, \tag{4.55}$$

where the dc gain Z_{io} is

$$Z_{io} = (1-D)^2 R_L + r \tag{4.56}$$

and the angular frequency of the left-half plane pole ω_{zvi} is

$$\omega_{zvi} = \frac{1}{C(R_L + r_C)}. \tag{4.57}$$

The gain Z_{ix} increases with frequency. Fig. 4.16 shows the theoretically obtained magnitude and phase plots of input impedance. The theoretical results were validated by simulation. Fig. 4.17 shows the magnitude and phase plots of input impedance using SABER Simulator.

4.4.7 Open-Loop Output Impedance Z_o

The small-signal model to derive output impedance is shown in Fig. 4.13. This model is obtain by setting $v_i = 0$ and $d = 0$. The open-loop output impedance is

$$Z_o(s) = \left.\frac{v_o(s)}{i_o(s)}\right|_{d=i_o=0} = \frac{Z_1}{(1-D)^2} || Z_2. \tag{4.58}$$

Substituting (4.24) and (4.25) in (4.58) gives the open-loop output impedance in s-domain as

$$Z_o(s) = \left.\frac{v_o(s)}{i_o(s)}\right|_{d=i_o=0} = Z_{ox}\frac{(s+\omega_{zn})(s+\omega_{rl})}{s^2 + 2\xi\omega_0 s + \omega_0^2} = Z_{o0}\frac{\left(1 + \frac{s}{\omega_{zn}}\right)\left(1 + \frac{s}{\omega_{rl}}\right)}{\left(\frac{s}{\omega_0}\right)^2 + \frac{2\xi s}{\omega_0} + 1}, \tag{4.59}$$

where the dc gain Z_{o0} is

$$Z_{o0} = \frac{rR_L}{r + (1-D)^2 R_L}, \tag{4.60}$$

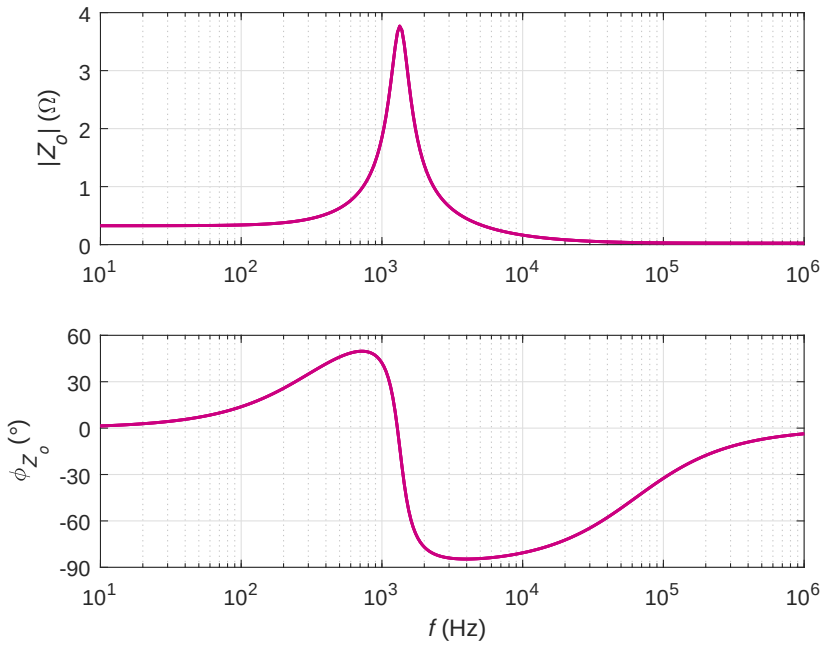

Figure 4.18: Theoretically obtained magnitude and phase plots of the output impedance Z_o.

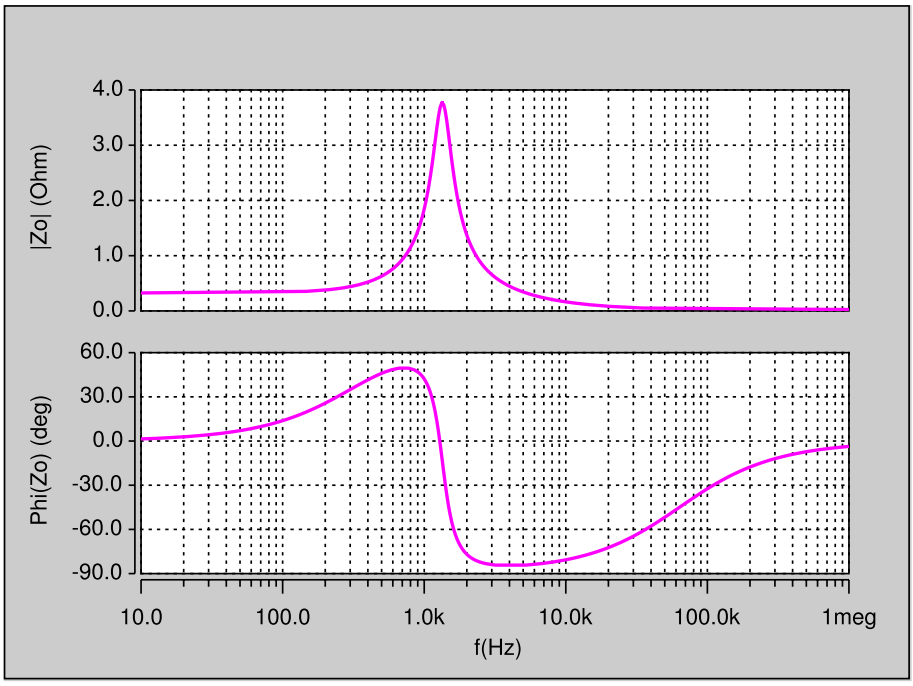

Figure 4.19: Magnitude and phase plots of the output impedance Z_o obtained by circuit simulation.

Table 4.2: Summary of calculated values for open-loop transfer functions

Variable	**Value**
$\lvert T_{po}\rvert$	30.38 dB
$\lvert T_{pio}\rvert$	8.94 dB
$\lvert M_{vo}\rvert$	4.44 dB
$\lvert M_{vio}\rvert$	-23.1 dB
$\lvert Z_{io}\rvert$	23.1 dB
$\lvert Z_{oo}\rvert$	-9.75 dB
ω_o	8.45 krad/s
f_o	1.35 kHz
ξ	0.163
ω_{zi}	500 rad/s
f_{zi}	80 Hz
ω_{zvi}	250 rad/s
f_{zvi}	40 kHz
ω_{zn}	400 krad/s
f_{zn}	63.66 kHz
ω_{zp}	281 krad/s
f_{zp}	45 kHz
ω_{rl}	2.32 krad/s
f_{rl}	370 Hz

the gain Z_{ox} is

$$Z_{ox} = \frac{R_L r_C}{R_L + r_C}, \tag{4.61}$$

and the angular frequency of the left-half plane zero ω_{rl} is

$$\omega_{rl} = \frac{r}{L}. \tag{4.62}$$

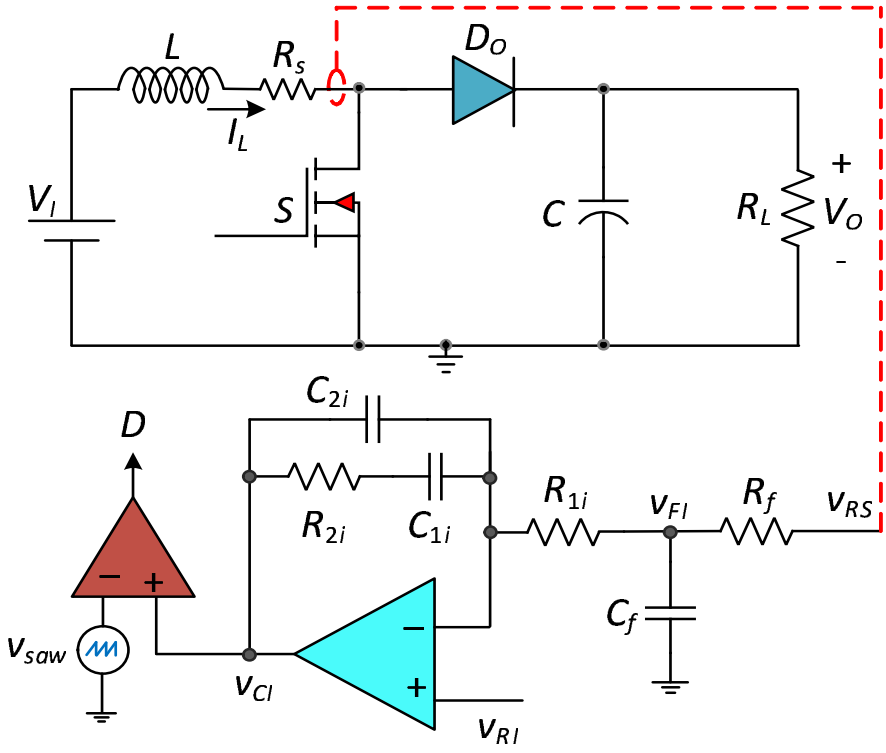

Figure 4.20: Circuit of boost dc-dc converter with inner-current loop.

The angular frequency of the left-half plane zero ω_{zn} is given in (4.32). Fig. 4.18 shows the theoretically obtained magnitude and phase plots of output impedance. The theoretical results were validated by simulation. Fig. 4.19 shows the magnitude and phase plots of output impedance using SABER Simulator.

4.5 Inner-Current Loop

Fig. 4.20 shows the circuit of boost dc-dc converter with inner-current loop. A sense resistor R_s is placed in the inductor branch to sense the inductor current and is a part of the feedback network. At low duty ratios, the sensed inductor current ripple is high. Therefore, the control voltage intersects with the modulator ramp voltage twice in each cycle resulting in subharmonic instability. The low-pass filter attenuates the switching frequency components and its harmonics present in the sensed voltage $v_{RS} = R_s i_L$. Therefore, the theoretically obtained output voltage of the low-pass

filter is $V_{FI} = R_s I_L$ and is governed by the dc component of the sensed inductor current. Thus, in this method the *true-average* component of the inductor current is sensed, thereby reducing the problems due to subharmonic instability and transistor misgating. The transfer functions related to the inner-current loop, which includes filter in the feedback path are derived and discussed in the following sections.

4.5.1 Design

The steady-state average inductor current is $I_L = V_O/[R_L(1-D)] = 0.833$ A. At a duty cycle $D = 0.4048$ and assuming the peak sawtooth voltage of the pulse-width modulator is $V_{Tm} = 3$ V, the required steady-state control voltage is $V_{CI} = DV_{Tm} = 0.4048 \times 3 = 1.2144$ V. The reference voltage to the current-loop is $V_{RI} = V_{CI}$ at steady-state since the error voltage is zero, i.e., $V_{RI} = 1.2144\ V$. The gain of the feedback path is controlled mainly by the sensor gain R_s such that $Tpicl \approx 1/Rs$. For a steady-state inductor current I_L and the inner loop reference voltage V_{RI}, which is assumed to be set by the outer voltage loop, the sense resistor can be determined using

$$R_s = \frac{V_{Rs}}{I_L} = \frac{V_{RI}}{I_L} = \frac{1.2144}{0.833} = 1.4573\ \Omega. \tag{4.63}$$

A standard resistor $R_s = 1.5\ \Omega$ was chosen.

4.5.2 Transfer Function of Filter T_f

The low-pass filter stage is composed of a resistor R_f and a capacitor C_f. The transfer function is

$$\begin{aligned} T_f(s) = \frac{v_{fi}(s)}{v_{rs}(s)} &= \frac{Z_{Cf}}{Z_{Cf} + R_f} = \frac{\dfrac{1}{sC_f}}{\dfrac{1}{sC_f} + R_f} = \frac{1}{1 + sR_fC_f} \\ &= \frac{1}{R_fC_f}\frac{1}{s + \dfrac{1}{R_fC_f}} = \frac{\omega_{pf}}{s + \omega_{pf}} = \frac{1}{\frac{s}{\omega_{pf}} + 1}. \end{aligned} \tag{4.64}$$

$$T_f(s) = \frac{1}{\frac{j\omega}{\omega_{pf}} + 1}, \tag{4.65}$$

Rearranging

$$T_f\left(\frac{j\omega + \omega_{pf}}{\omega_{pf}}\right) = 1, \tag{4.66}$$

$$T_f(j\omega + \omega_{pf}) = \omega_{pf}, \tag{4.67}$$

Further modifications results in

$$\omega_{pf} = \frac{jT_f\omega}{1 - T_f} \tag{4.68}$$

and hence

$$f_{pf} = \frac{jT_f f}{1 - T_f}. \tag{4.69}$$

Therefore, the filter upper cutoff frequency can be obtained as

$$f_{pf} = \sqrt{\frac{(T_f f)^2}{(1 - T_f)^2}} = \frac{T_f f}{1 - T_f}. \tag{4.70}$$

The filter frequency can be set by the amount of attenuation desired. For an example, to achieve an attenuation of 33% in the filter output voltage at the switching frequency, i.e., $|T_f|(f_s) = 0.33$, the filter upper cutoff frequency using (4.70) must be $f_{pf} = 0.5f_s = 50$ kHz. The filter resistance is chosen as $R_f = 1$ kΩ and the filter capacitance is calculated as $C_f = 3.183$ nF.

4.5.3 Transfer Function of Pulse-Width Modulator T_m

The control voltage-to-duty cycle transfer function of the pulse-width modulator is

$$T_m = \frac{D}{V_C} = \frac{d}{v_c} = \frac{1}{V_{Tm}}, \tag{4.71}$$

where V_{Tm} is the amplitude of the sawtooth waveform.

4.5.4 Uncompensated Loop Gain T_{ki}

The natural behavior of the inner current loop can be determined using the uncompensated loop gain as

$$T_{ki} = \frac{v_{fi}}{v_{ei}} = T_m T_{pi} R_s T_f = T_{ki0} \frac{\left(1 + \frac{s}{\omega_{zi}}\right)}{\left(1 + \frac{s}{\omega_{pf}}\right)\left(1 + \frac{2\xi s}{\omega_0} + \frac{s^2}{\omega_0^2}\right)}, \tag{4.72}$$

where T_m, T_{pi} and T_f are given in (4.71), (4.36), and (4.64), respectively. The dc gain T_{ki0} is given by

$$T_{ki0} = \frac{R_s}{V_{Tm}} \frac{V_I}{R_L + r}. \tag{4.73}$$

Fig. 4.21 shows the theoretically obtained magnitude and phase plots of the uncompensated loop gain of the inner-current loop.

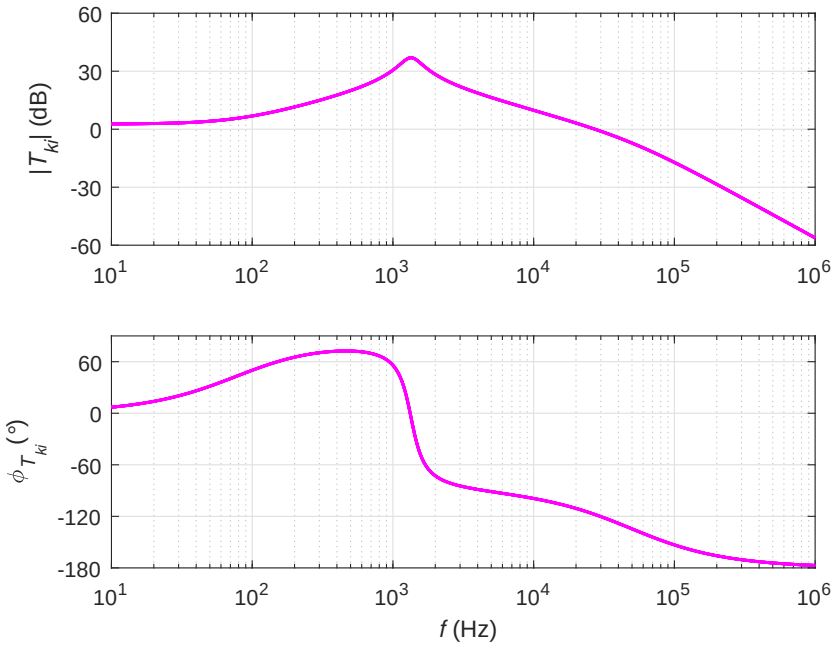

Figure 4.21: Theoretically obtained magnitude and phase plots of the uncompensated loop gain T_{ki} of inner-current loop.

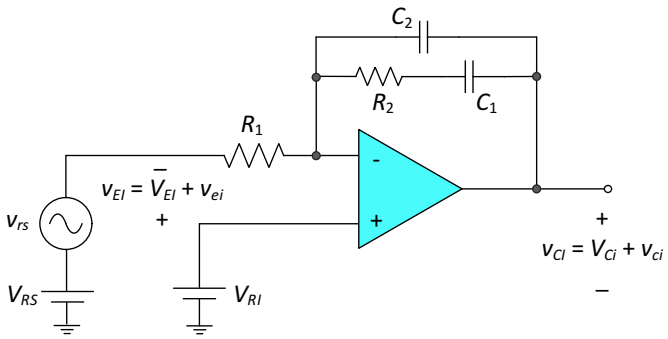

Figure 4.22: Circuit of Type-II compensator.

4.5.5 Transfer Function of Control Circuit T_{ci}

An integral single-lead control circuit introduces a pole at the origin required to boost the dc gain and a pole-zero pair to adjust crossover frequency f_c to maintain a required phase margin (PM). A detailed procedure to determine the transfer function of the controller to improve the dc gain (> 50 dB) and achieve an inner current loop phase

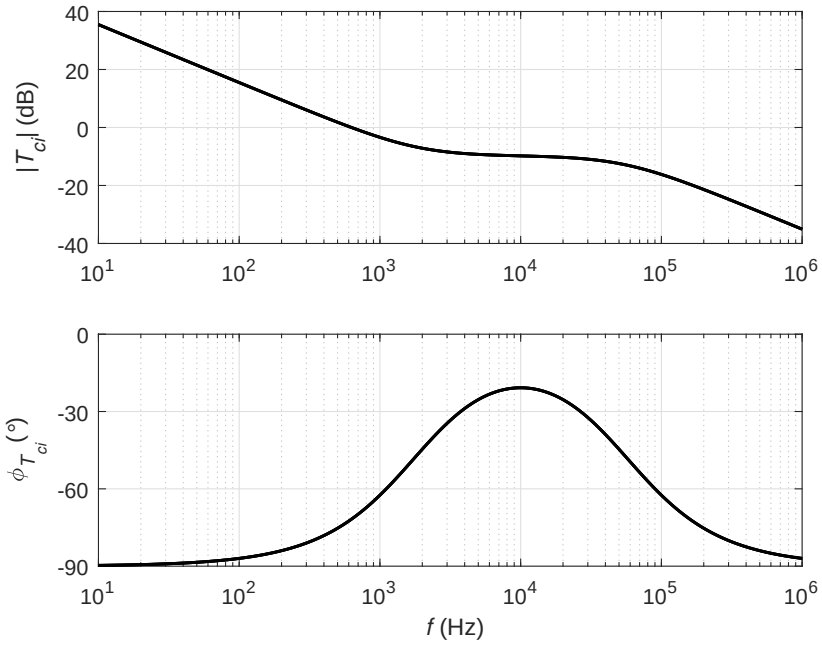

Figure 4.23: Theoretically obtained magnitude and phase plots of controller transfer function T_{ci} for the inner-current loop.

margin $PM = 60°$ is explained in [34] and only the relevant expressions are presented here. The transfer function T_{ci} of the current loop control circuit is

$$T_{ci} = \frac{v_{ci}(s)}{v_{ei}(s)} = T_{cio} \frac{1 + \dfrac{s}{\omega_{zci}}}{s\left(1 + \dfrac{s}{\omega_{pci}}\right)}, \tag{4.74}$$

where

$$T_{cio} = \frac{1}{R_1(C_1 + C_2)}, \tag{4.75}$$

$$\omega_{zci} = \frac{1}{R_2 C_1}, \tag{4.76}$$

and

$$\omega_{zci} = \frac{(C_1 + C_2)}{R_2 C_1 C_2}. \tag{4.77}$$

Fig. 4.23 shows the theoretically obtained magnitude and phase plots of the compensator transfer function used in the inner-current loop. The theoretical results

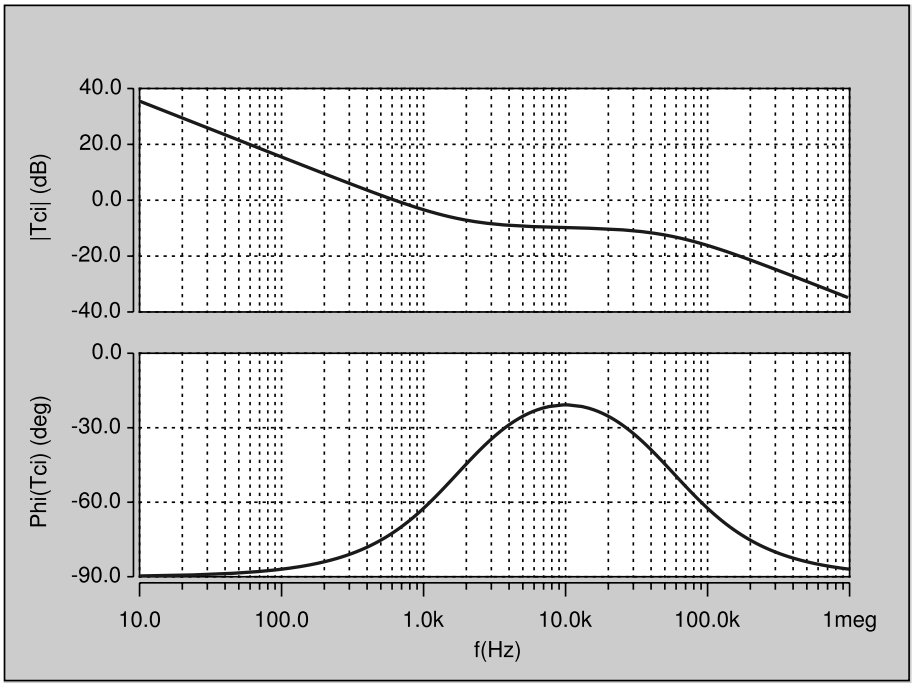

Figure 4.24: Magnitude and phase plots of output impedance obtained by circuit simulation of controller transfer function T_{ci} for the inner-current loop.

were validated by simulation. Fig. 4.24 shows the magnitude and phase plots of the compensator transfer function used in the inner-current loop using SABER Simulator.

4.5.6 Loop Gain of Inner-Current Loop T_i

The loop gain of the compensated inner-current loop is

$$T_i = \frac{v_{ei}}{v_{fi}} = T_{ki}T_{ci} = T_m T_{pi} R_s T_f T_{ci}, \tag{4.78}$$

to yield

$$T_i = T_{i0} \frac{\left(1 + \frac{s}{\omega_{zi}}\right)\left(1 + \frac{s}{\omega_{zci}}\right)}{s\left(1 + \frac{s}{\omega_{pf}}\right)\left(1 + \frac{s}{\omega_{pci}}\right)\left(1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}\right)}, \tag{4.79}$$

where T_{i0} is the gain at $s = 0$ given as

$$T_{i0} = T_{ki0}T_{ci0} = \frac{V_I R_s}{V_{Tm}(R_L + r)} \frac{1}{R_1(C_1 + C_2)}. \tag{4.80}$$

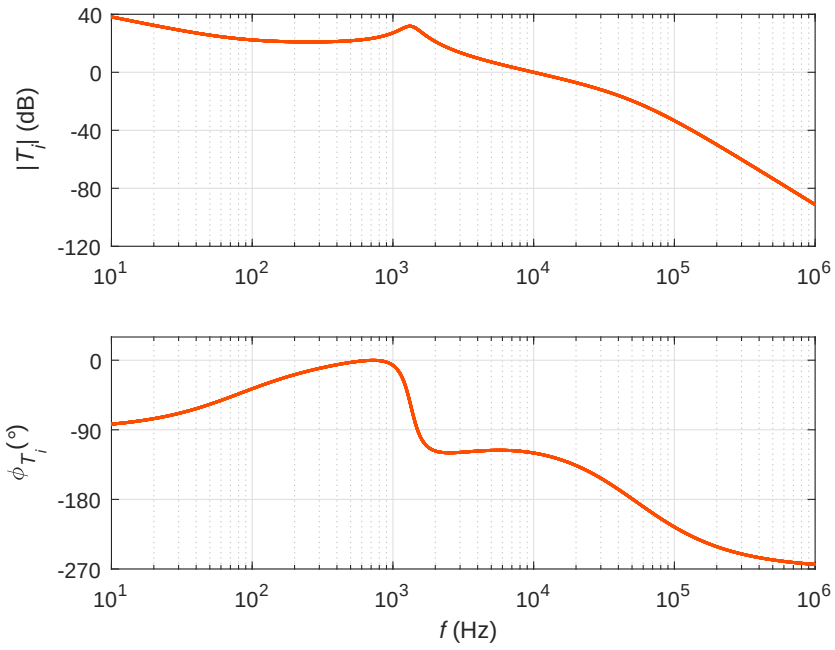

Figure 4.25: Theoretically obtained magnitude and phase plots of compensated loop gain T_i of the inner-current loop.

Fig. 4.25 shows the theoretically obtained magnitude and phase plots of loop gain of the inner-current loop. The theoretical results were validated by simulation. Fig. 4.26 shows the magnitude and phase plots of loop gain of the inner-current loop using SABER Simulator.

4.6 Closed-Loop Transfer Functions for Inner-Current Loop

The following closed-loop control transfer functions are derived:

- Reference voltage-to-inductor current transfer function T_{icl}
- Reference voltage-to-output voltage transfer function T_{picl}
- Input voltage-to-inductor current transfer function M_{icl}
- Input voltage-to-output voltage transfer function M_{vicl}
- Input voltage-to-duty cycle transfer function M_{di}

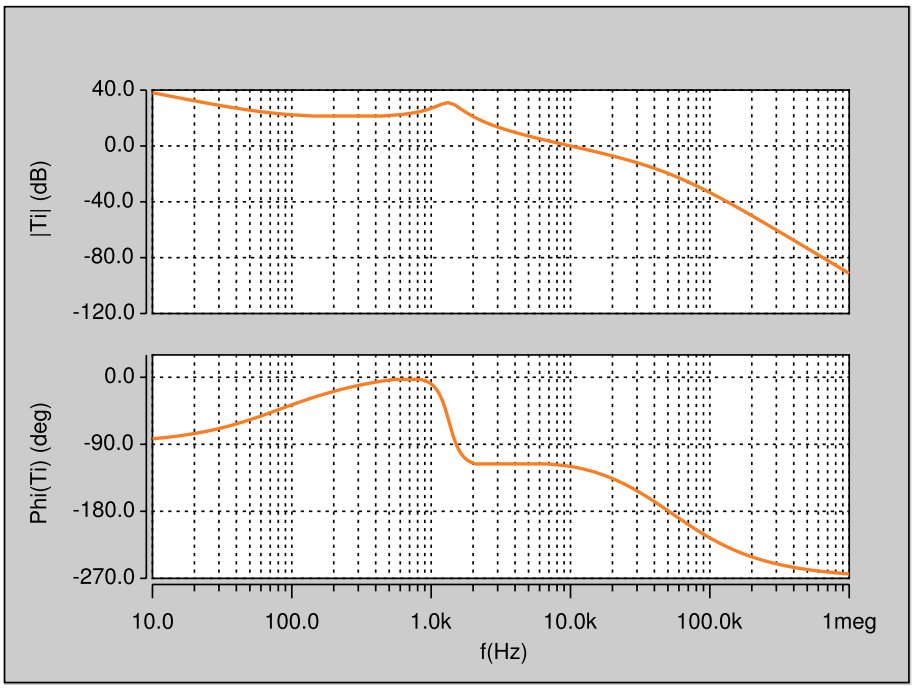

Figure 4.26: Magnitude and phase plots of compensated loop gain T_i of the inner-current loop obtained by circuit simulation.

- Input impedance Z_{iicl}
- Output impedance Z_{oicl}

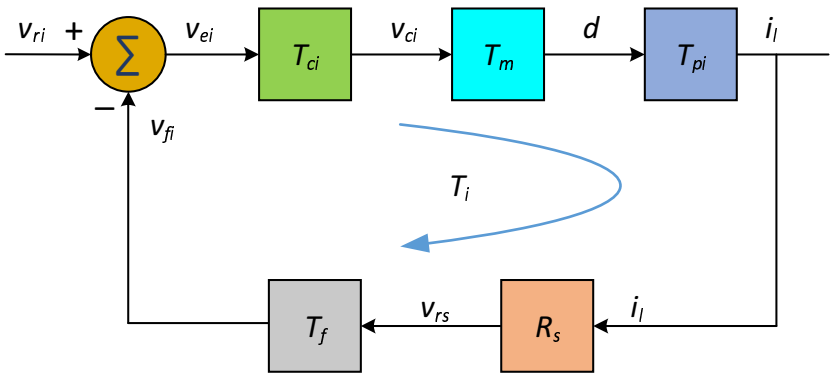

Figure 4.27: Block diagram used to derive inner-loop control-to-inductor current transfer function T_{icl}.

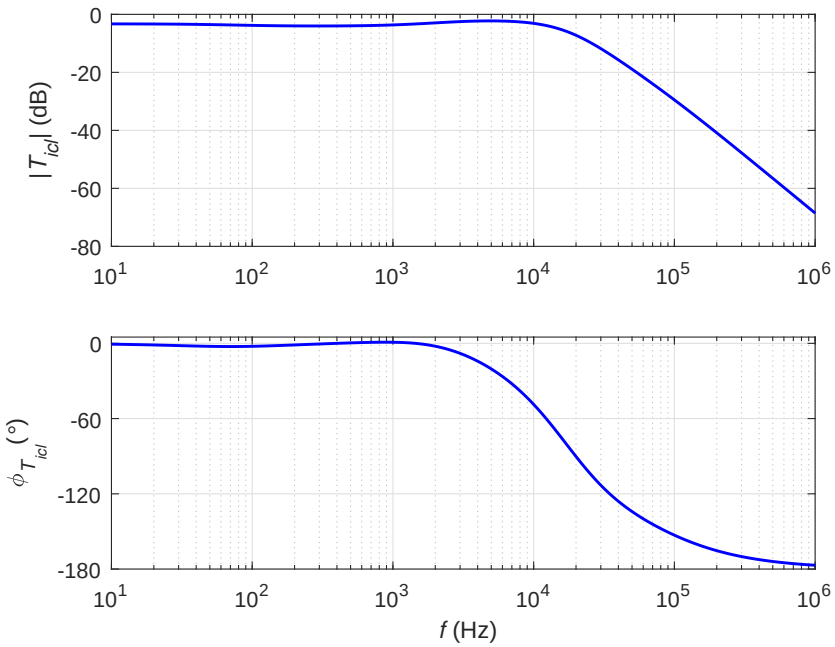

Figure 4.28: Theoretically obtained magnitude and phase plots of the inner-current loop reference voltage-to-inductor current transfer function T_{icl}.

4.6.1 Reference Voltage-to-Inductor Current Transfer Function T_{icl}

Using the block diagram shown in Fig. 4.27, the closed-loop reference voltage-to-inductor current transfer function is

$$T_{icl}(s) = \left.\frac{i_l(s)}{v_{ri}(s)}\right|_{v_i=i_o=0} = \frac{T_{ci}T_mT_{pi}}{1+T_i}. \tag{4.81}$$

Fig. 4.28 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop reference voltage-to-inductor current transfer function. The theoretical results were validated by simulation. Fig. 4.29 shows the magnitude and phase plots of the inner-current loop reference voltage-to-inductor current transfer function using SABER Simulator.

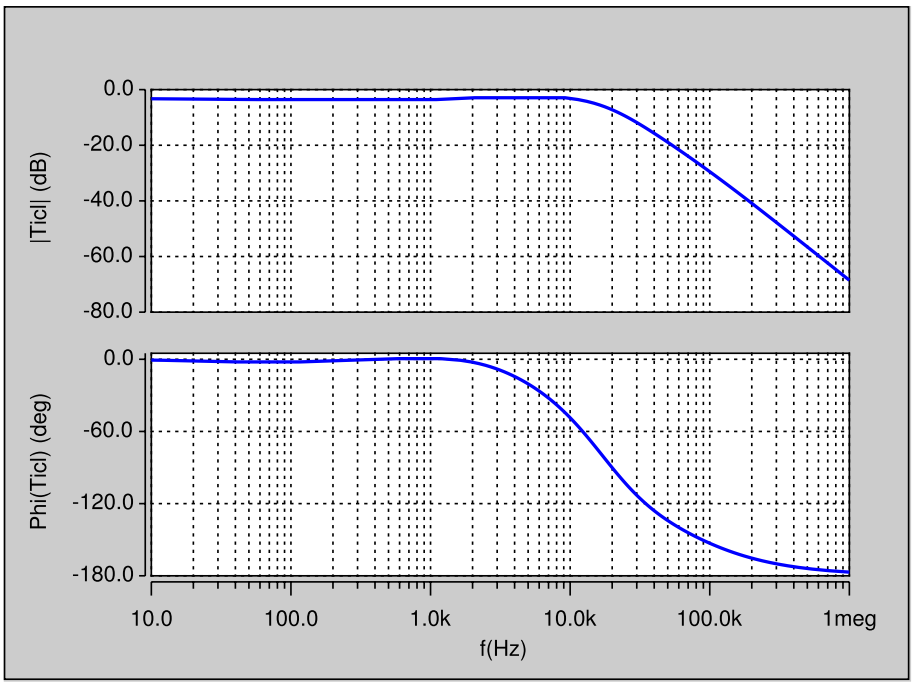

Figure 4.29: Magnitude and phase plots of the inner-current loop reference voltage-to-inductor current transfer function T_{icl} obtained by circuit simulation.

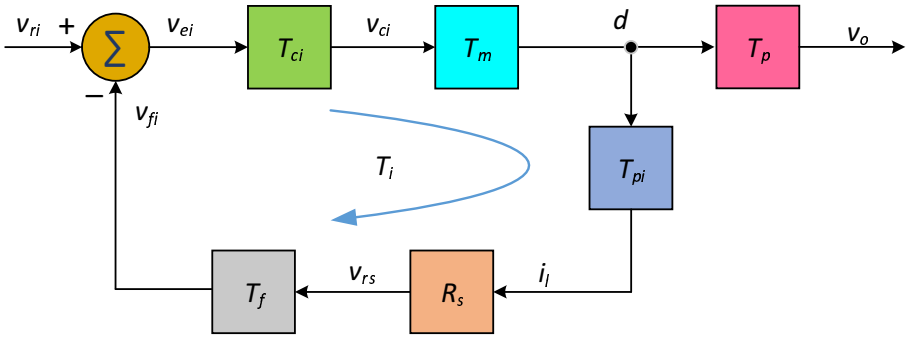

Figure 4.30: Block diagram required to derive inner-loop control-to-output voltage transfer function T_{picl}.

4.6.2 Reference Voltage-to-Output Voltage Transfer Function T_{picl}

Using the block diagram shown in Fig. 4.30, the closed-loop reference voltage-to-output voltage transfer function is

$$T_{picl}(s) = \left.\frac{v_o(s)}{v_{ri}(s)}\right|_{v_i=i_o=0} = \frac{T_{ci}T_mT_p}{1+T_i}. \tag{4.82}$$

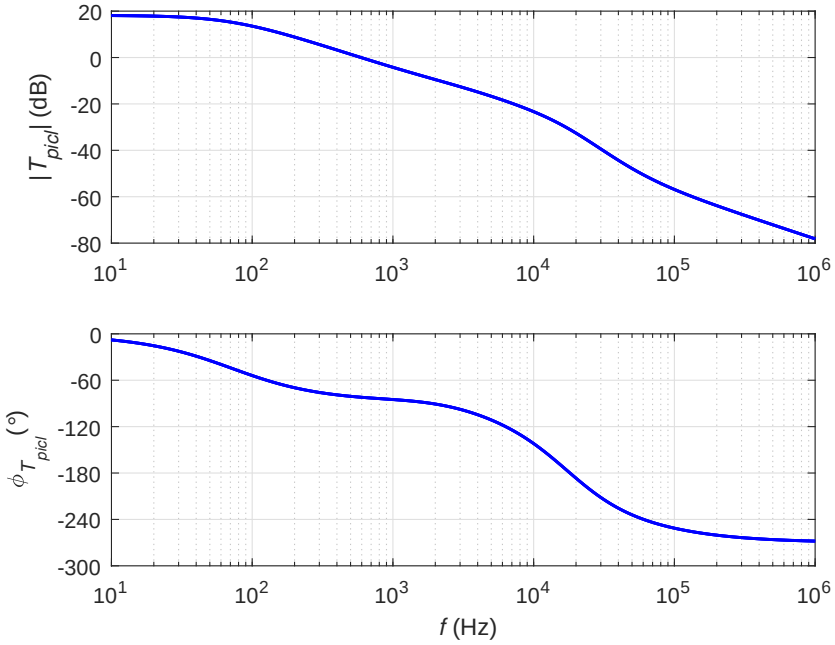

Figure 4.31: Theoretically obtained magnitude and phase plots of reference voltage-to-output voltage transfer function T_{picl}.

Fig. 4.31 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop reference voltage-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 4.32 shows the magnitude and phase plots of the inner-current loop reference voltage-to-output voltage transfer function using SABER Simulator.

4.6.3 Input Voltage-to-Inductor Current Transfer Function M_{icl}

Using the block diagram shown in Fig. 4.33, the closed-loop input voltage-to-inductor current transfer function is

$$M_{icl}(s) = \left.\frac{i_l(s)}{v_i(s)}\right|_{v_{ri}=i_o=0}. \tag{4.83}$$

From the block diagram,

$$i_l = i_l' + i_l'' = -T_{ci}T_mT_{pi}T_fR_si_l + M_{vi}v_i = (-T_i)i_l + M_{vi}v_i, \tag{4.84}$$

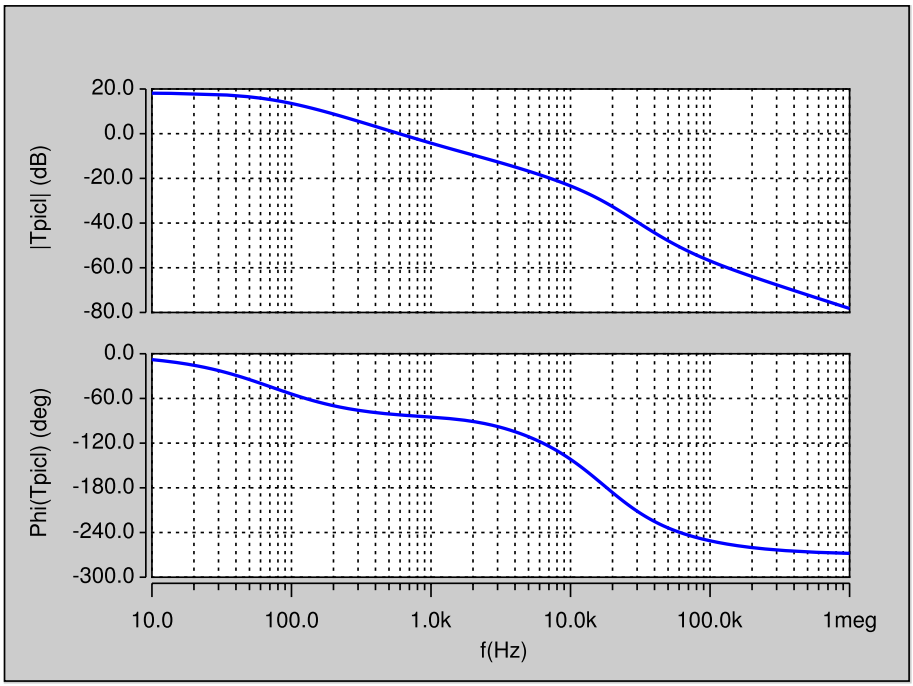

Figure 4.32: Magnitude and phase plots ofReference voltage-to-output voltage transfer function T_{picl} obtained by circuit simulation.

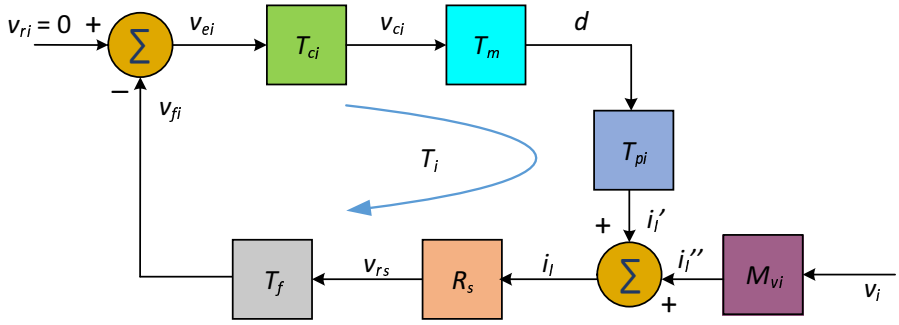

Figure 4.33: Block diagram required to derive inner-loop input voltage-to-inductor current transfer function M_{icl}.

$$i_l(1 + T_i) = M_{vi} v_i. \tag{4.85}$$

Hence

$$M_{icl}(s) = \frac{i_l(s)}{v_i(s)} = \frac{M_{vi}}{1 + T_i}. \tag{4.86}$$

Fig. 4.34 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop input voltage-to-inductor current transfer

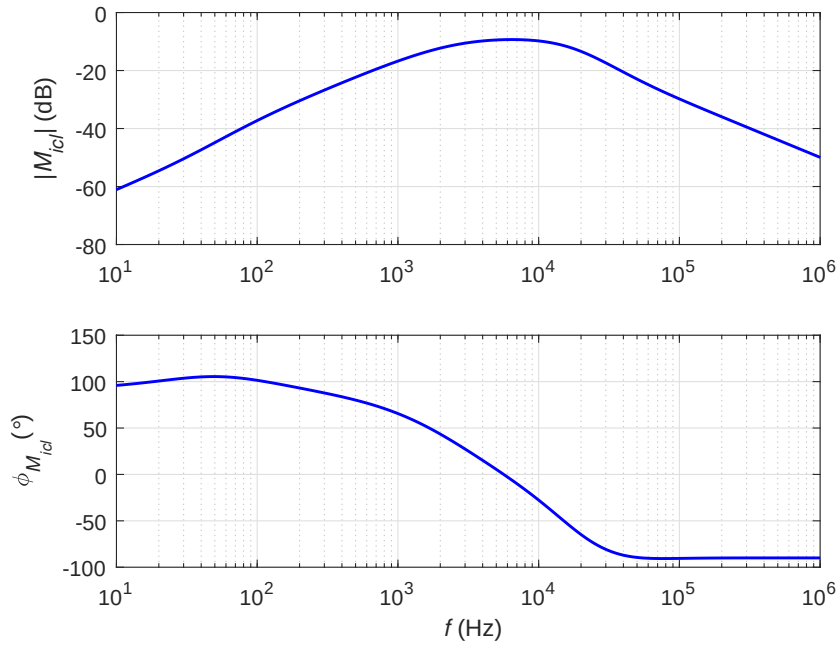

Figure 4.34: Theoretically obtained magnitude and phase plots of input voltage-to-inductor current transfer function M_{icl}.

function. The theoretical results were validated by simulation. Fig. 4.35 shows the magnitude and phase plots of the inner-current loop input voltage-to-inductor current transfer function using SABER Simulator.

4.6.4 Input Voltage-to-Output Voltage Transfer Function M_{vicl}

Using the block diagram shown in Fig. 4.36, the closed-loop input voltage-to-output voltage transfer function is

$$M_{vicl}(s) = \left.\frac{v_o(s)}{v_i(s)}\right|_{v_{ri}=i_o=0}, \tag{4.87}$$

From the block diagram

$$i_l = i_l' + i_l'' = T_{pi}d + M_{vi}v_i. \tag{4.88}$$

$$\frac{-d}{T_{ix}} = T_{pi}d + M_{vi}v_i, \tag{4.89}$$

where

$$T_{ix} = \frac{T_i}{T_{pi}}. \tag{4.90}$$

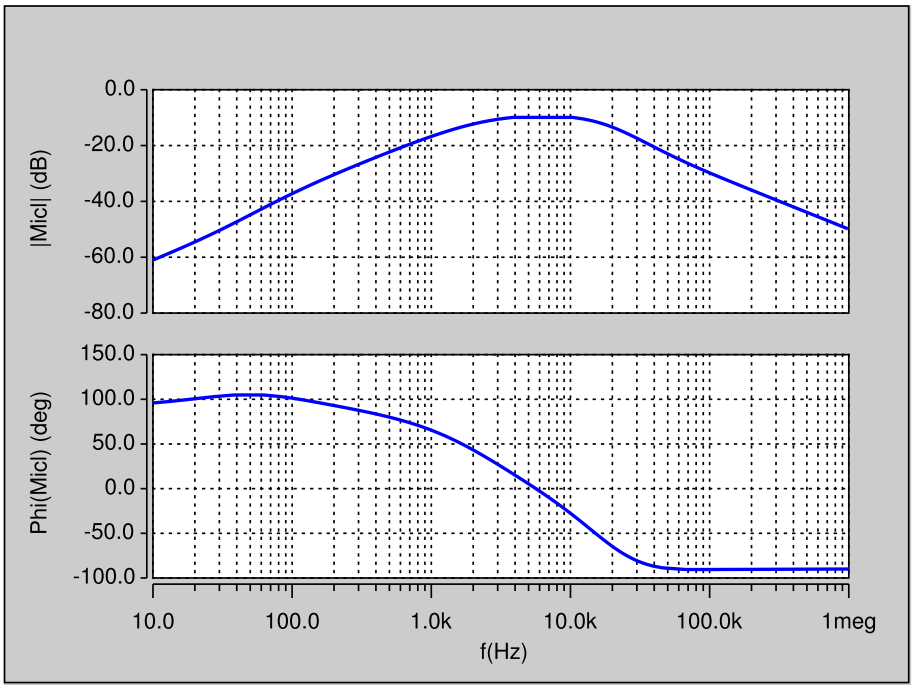

Figure 4.35: Magnitude and phase plots of input voltage-to-inductor current transfer function M_{icl} obtained by circuit simulation.

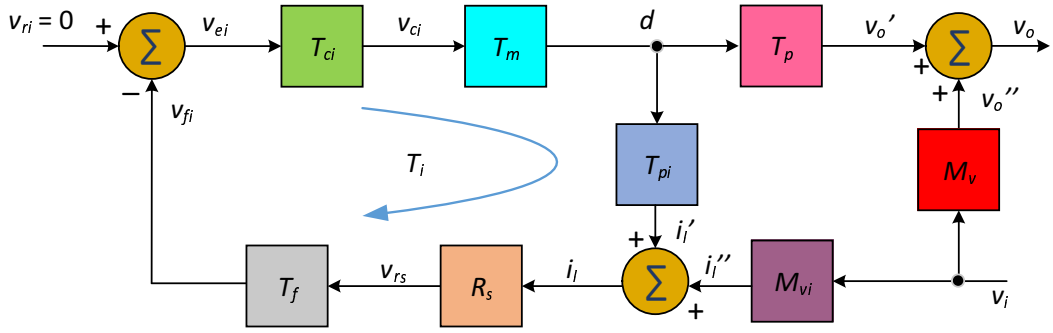

Figure 4.36: Block diagram required to derive inner-loop input voltage-to-output voltage transfer function M_{vicl}.

Rearranging

$$-d\left(\frac{1}{T_{ix}} + T_{pi}\right) = M_{vi}v_i. \tag{4.91}$$

$$-d\left(\frac{1 + T_{ix}T_{pi}}{T_{ix}}\right) = M_{vi}v_i. \tag{4.92}$$

$$d = -\frac{M_{vi}T_{ix}}{1 + T_i}v_i. \tag{4.93}$$

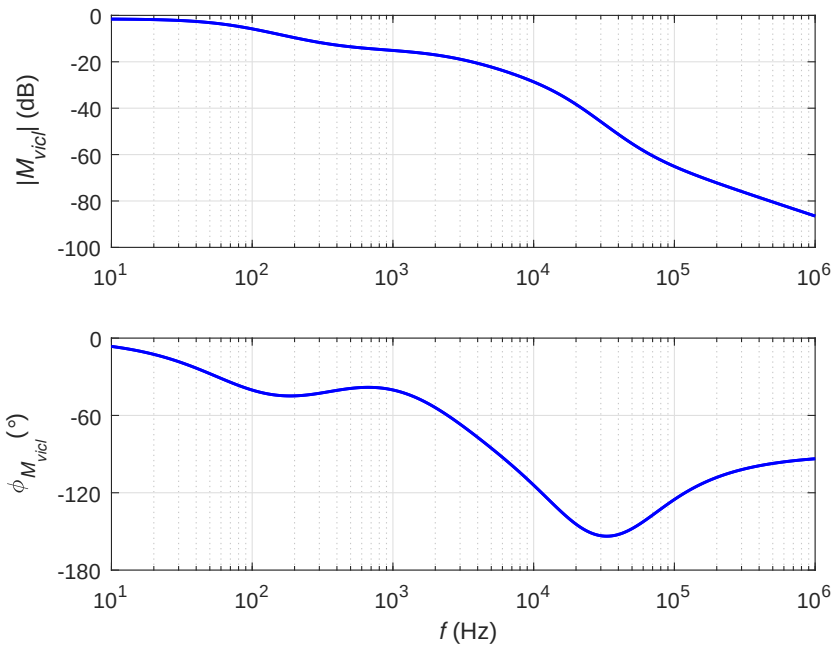

Figure 4.37: Theoretically obtained magnitude and phase plots of input voltage-to-output voltage transfer function transfer function M_{vicl}.

From the block diagram in Fig. (4.36)

$$v_o = v_o' + v_o'' = T_p d + M_v v_i. \tag{4.94}$$

Substituting d from (4.93), we get

$$v_o = T_p\left(- \frac{M_{vi}T_{ix}}{1+T_i}v_i\right) + M_v v_i. = \left(M_v - \frac{T_p M_{vi}T_{ix}}{1+T_i}\right)v_i. \tag{4.95}$$

The closed-loop input-to-output transfer function is

$$M_{vicl}(s) = \frac{v_o(s)}{v_i(s)} = M_v(1+T_i) - \frac{T_p M_{vi}T_{ix}}{1+T_i}. \tag{4.96}$$

Fig. 4.37 shows the theoretically obtained magnitude and phase plots of inner-current loop input voltage-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 4.38 shows the magnitude and phase plots of the inner-current loop input voltage-to-output voltage transfer function using SABER Simulator.

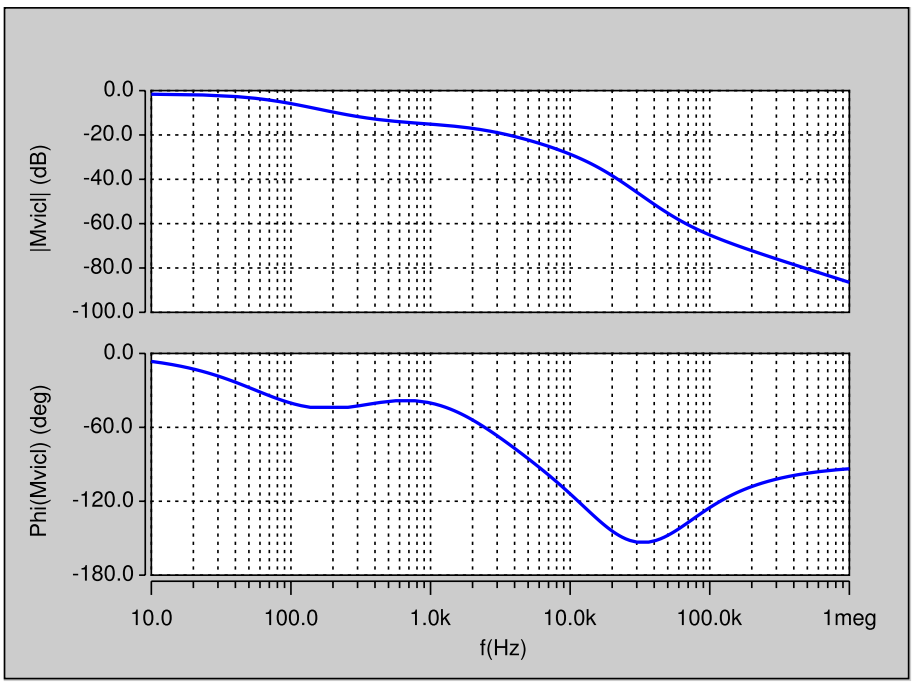

Figure 4.38: Magnitude and phase plots of input voltage-to-output voltage transfer function transfer function M_{vicl} obtained by circuit simulation.

4.6.5 Input Voltage-to-Duty Cycle Transfer Function M_{di}

Using the block diagram shown in Fig. 4.36, the closed-loop input voltage to duty cycle transfer function is

$$M_{di}(s) = \left.\frac{d(s)}{v_i(s)}\right|_{v_{ri}=i_o=0}. \tag{4.97}$$

From (4.93)

$$d = -\frac{M_{vi}T_{ix}}{1+T_i}v_i. \tag{4.98}$$

Hence the closed-loop input voltage to duty-cycle transfer function is

$$M_{di}(s) = \frac{d(s)}{v_i(s)} = -\frac{M_{vi}T_{ix}}{1+T_i} = -\frac{M_{vi}}{T_{pi}}\frac{T_i}{1+T_i}. \tag{4.99}$$

Fig. 4.39 shows the theoretically obtained magnitude and phase plots of the inner-current loop input voltage-to-duty cycle transfer function. The theoretical results were validated by simulation. Fig. 4.40 shows the magnitude and phase plots of

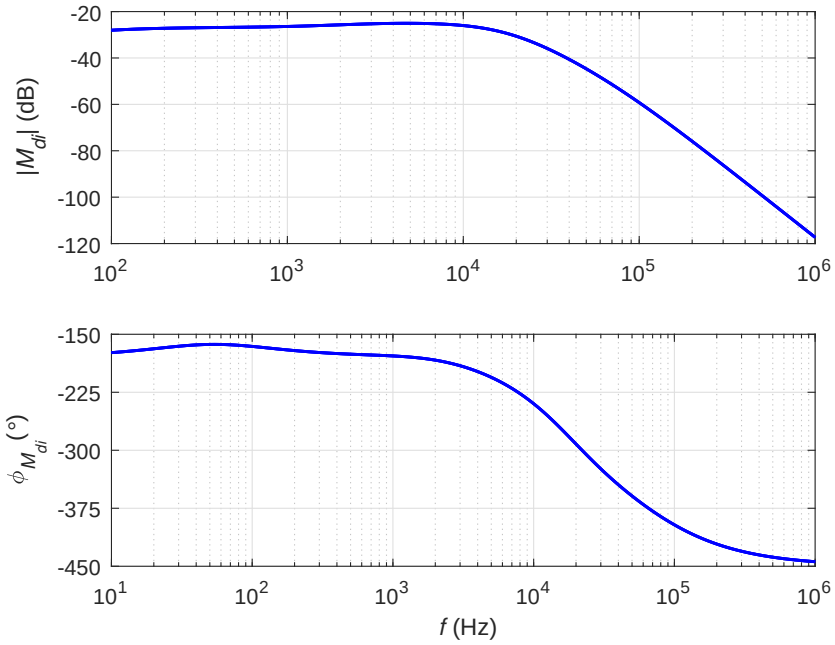

Figure 4.39: Theoretically obtained magnitude and phase plots of input voltage-to-duty cycle transfer function M_{di}

the inner-current loop input voltage-to-duty cycle transfer function using SABER Simulator.

4.6.6 Input Impedance Z_{iicl}

The closed-inner-loop input impedance is

$$Z_{iicl}(s) = \left.\frac{v_i(s)}{i_i(s)}\right|_{i_o=v_{ri}=0}. \tag{4.100}$$

From Fig. 4.41, the inductor current is

$$i_l = i_l' + i_l'' = T_{pi}d + M_{vi}v_i \tag{4.101}$$

and the duty cycle is

$$d = T_{ci}T_m v_{ei} = T_{ci}T_m(-T_f R_s i_l). \tag{4.102}$$

Substituting (4.102) in (4.101)

$$i_l = -T_{pi}T_{ci}T_m T_f R_s i_l + M_{vi}v_i = -T_i i_l + M_{vi}v_i. \tag{4.103}$$

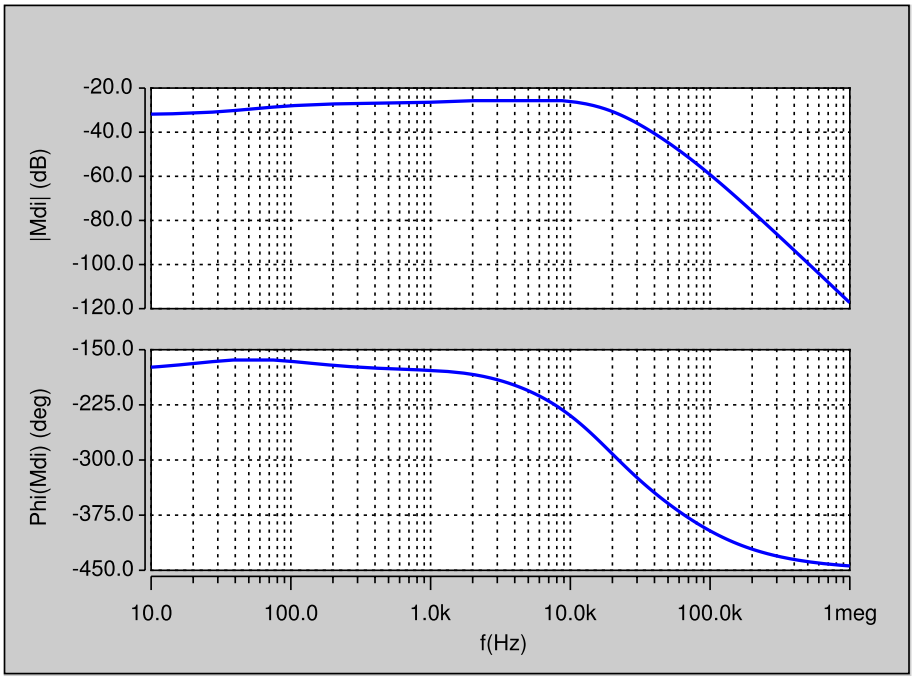

Figure 4.40: Magnitude and phase plots of input voltage-to-duty cycle transfer function M_{di} obtained by circuit simulation.

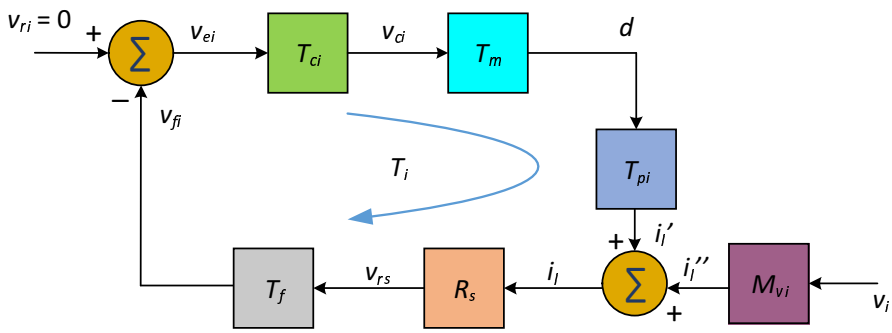

Figure 4.41: Block diagram used to derive inner-closed loop input impeance Z_{iicl}.

Rearranging (4.103)

$$i_l = \frac{M_{vi}}{1 + T_i} v_i. \tag{4.104}$$

The input current is given as

$$i_i = i_l = \frac{M_{vi}}{1 + T_i} v_i. \tag{4.105}$$

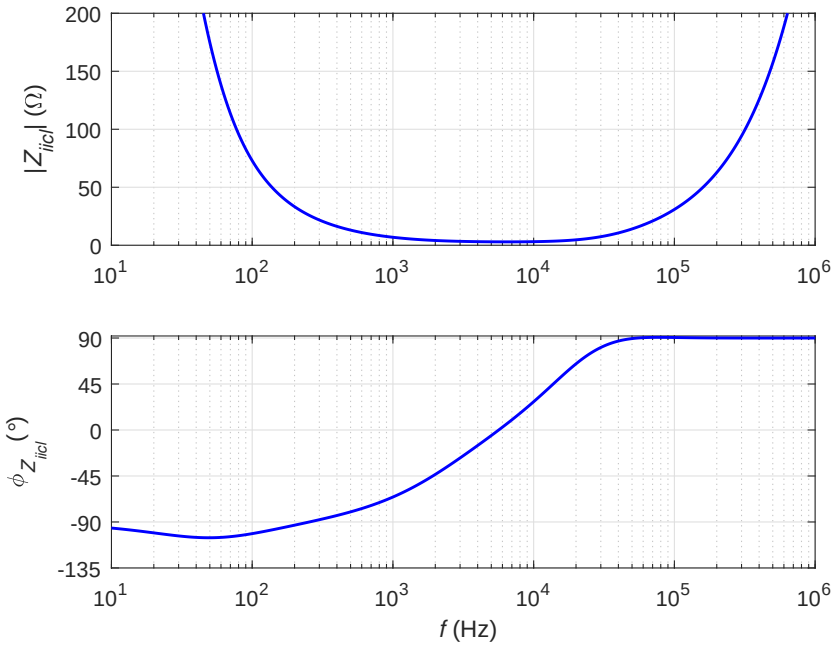

Figure 4.42: Theoretically obtained magnitude and phase plots of inner-loop input impedance Z_{iicl}.

The closed-loop input admittance is

$$Y_{iicl}(s) = \frac{i_i(s)}{v_i(s)} = \frac{M_{vi}}{1 + T_i}. \tag{4.106}$$

For boost converter

$$M_{vi} = \frac{i_i}{v_i} = \frac{i_l}{v_i} = \frac{1}{Z_i} = Y_i. \tag{4.107}$$

Hence, the closed-inner-loop input impedance is

$$Z_{iicl}(s) = \left.\frac{v_i(s)}{i_i(s)}\right|_{i_o = v_{ri} = 0} = \frac{1}{Y_{iicl}} = Z_i(1 + T_i). \tag{4.108}$$

Fig. 4.42 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop input impedance. The theoretical results were validated by simulation. Fig. 4.43 shows the magnitude and phase plots of the inner-current loop input impedance using SABER Simulator.

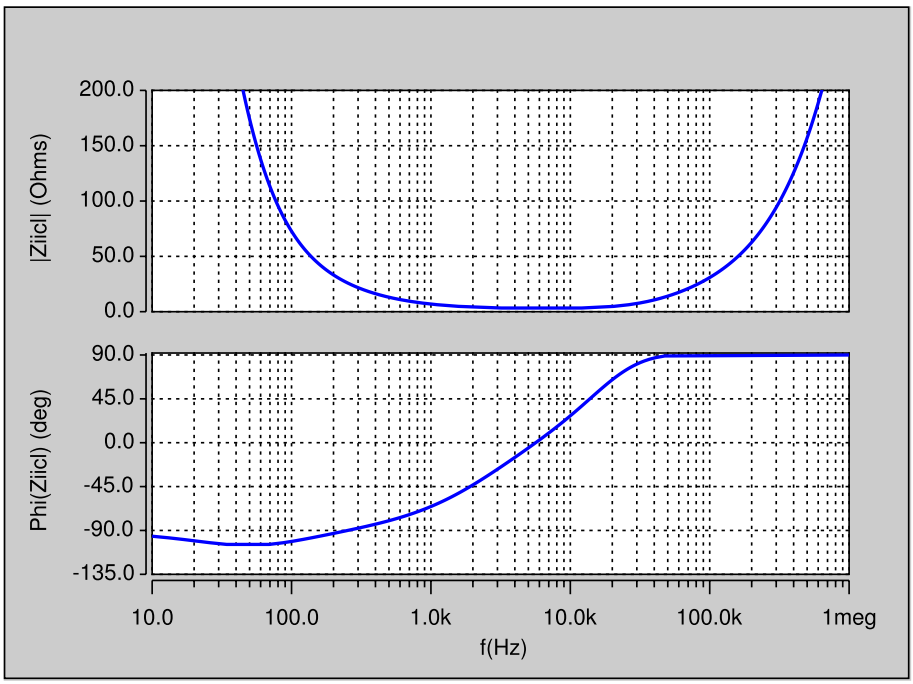

Figure 4.43: Magnitude and phase plots of inner-loop input impedance Z_{iicl} obtained by circuit simulation.

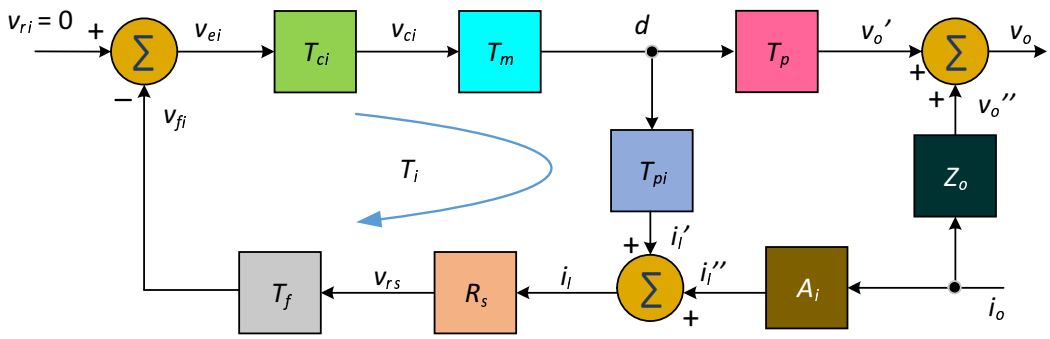

Figure 4.44: Block diagram required to derive inner-closed-loop input impedance Z_{oicl}.

4.6.7 Output Impedance Z_{oicl}

Using the block diagram shown in Fig. 4.44, the closed-inner loop output impedance is

$$Z_{oicl}(s) = \left.\frac{v_o(s)}{i_o(s)}\right|_{v_{ri}=v_i=0}. \tag{4.109}$$

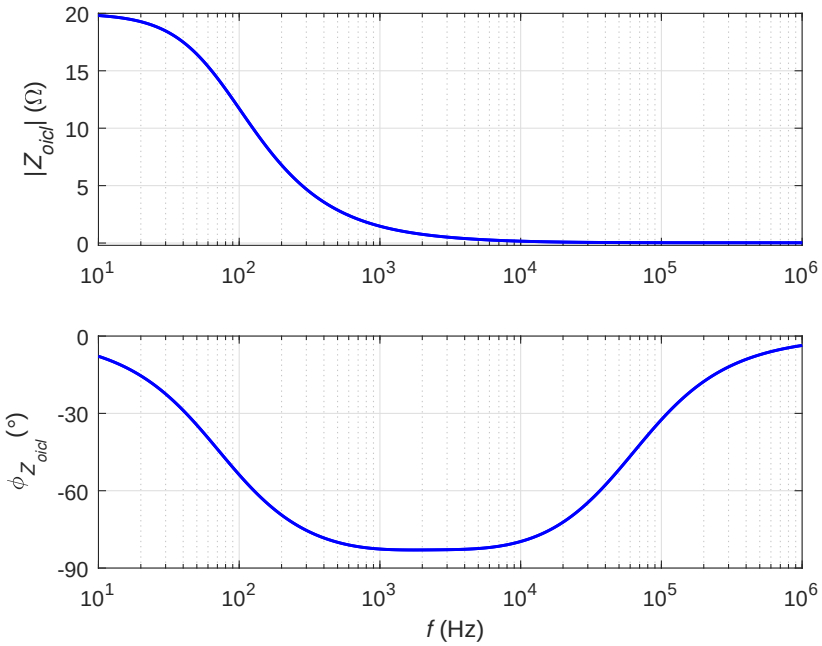

Figure 4.45: Theoretically obtained magnitude and phase plots of inner-closed loop output impedance Z_{oicl}.

From the block diagram

$$i_l = i_l' + i_l'' = T_{pi}d + A_i i_o \tag{4.110}$$

and

$$\frac{-d}{T_{ix}} = T_{pi}d + A_i i_o \tag{4.111}$$

Rearranging

$$-d\left(\frac{1}{T_{ix}} + T_{pi}\right) = A_i i_o. \tag{4.112}$$

and

$$d = -\frac{A_i T_{ix}}{1 + T_i} i_o. \tag{4.113}$$

From the block diagram in Fig. (4.44)

$$v_o = v_o' + v_o'' = T_p d + Z_o i_o. \tag{4.114}$$

Substituting d from (4.93), we get

$$v_o = T_p\left(-\frac{A_i T_{ix}}{1 + T_i} i_o\right) + Z_o i_o. = \left(Z_o - \frac{A_i T_p T_{ix}}{1 + T_i}\right) i_o. \tag{4.115}$$

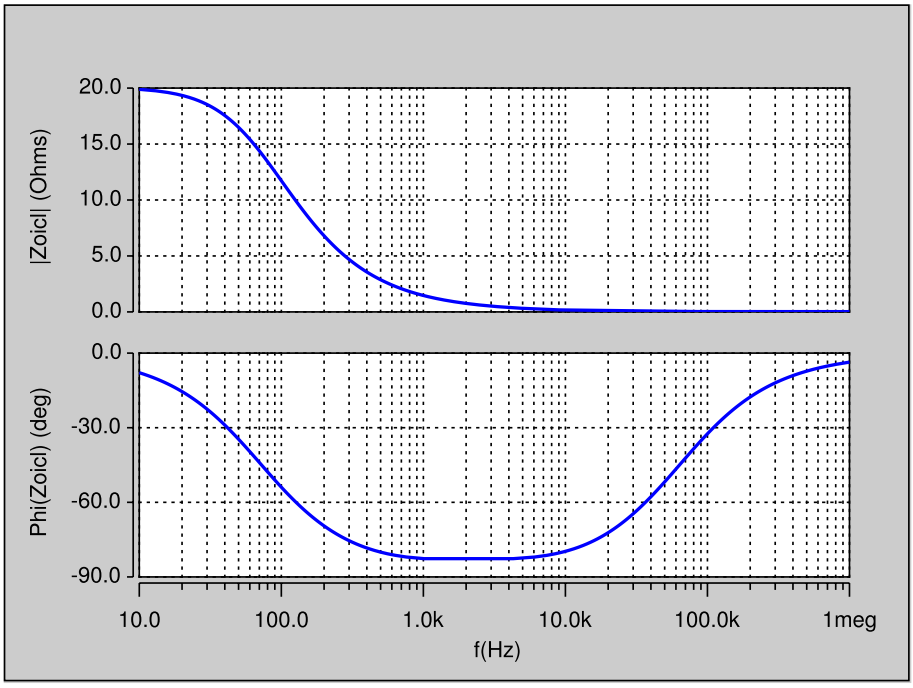

Figure 4.46: Magnitude and phase plots of inner-closed loop output impedance Z_{oicl} obtained by simulations.

The closed-inner loop output impedance is

$$Z_{oicl}(s) = \frac{v_o(s)}{i_o(s)} = Z_o - \frac{A_i T_p T_{ix}}{1 + T_i}. \tag{4.116}$$

Fig. 4.45 shows the theoretically obtained magnitude and phase plots of the inner-current loop output impedance. The theoretical results were validated by simulation. Fig. 4.46 shows the magnitude and phase plots of the inner-current loop output impedance using SABER Simulator.

4.7 Outer-Voltage Loop

4.7.1 Uncompensated Loop Gain for Outer-Voltage Loop T_{kv}

The natural behavior of the outer-voltage loop is determined using the uncompensated loop gain as

$$T_{kv} = \frac{v_{fv}}{v_{ev}} = \frac{\beta v_o}{v_{ri}} = \beta T_{picl} = \frac{\beta T_{ci} T_m T_p}{1 + T_i}. \tag{4.117}$$

4.7.2 Transfer Function of Control Circuit for Outer-Voltage Loop T_{cv}

An integral-single-lead control circuit introduces a pole at the origin required to boost the dc gain and a pole-zero pair to adjust crossover frequency f_c to maintain required PM. A detailed procedure to determine the transfer function of the controller to improve the dc gain ($>$ 50 dB) and achieve an inner current loop phase margin $PM = 60^\circ$ is explained in [34] and only the relevant expressions are presented here. The transfer function T_{ci} of the current loop control circuit is

$$T_{cv} = \frac{v_{cv}(s)}{v_{ev}(s)} = T_{cvo} \frac{1 + \frac{s}{\omega_{zcv}}}{s\left(1 + \frac{s}{\omega_{pcv}}\right)}, \tag{4.118}$$

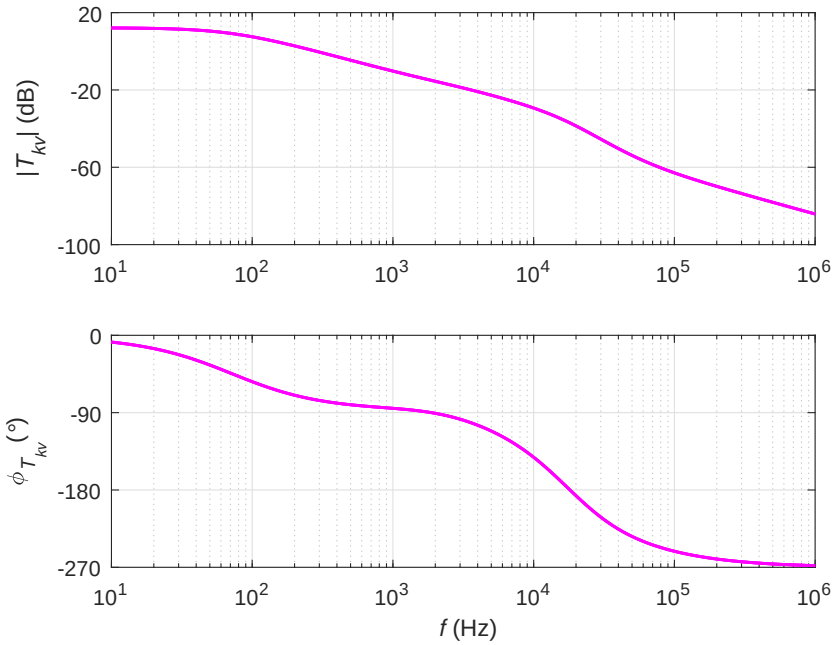

Figure 4.47: Theoretically obtained magnitude and phase plots of uncompensated loop gain T_{kv}.

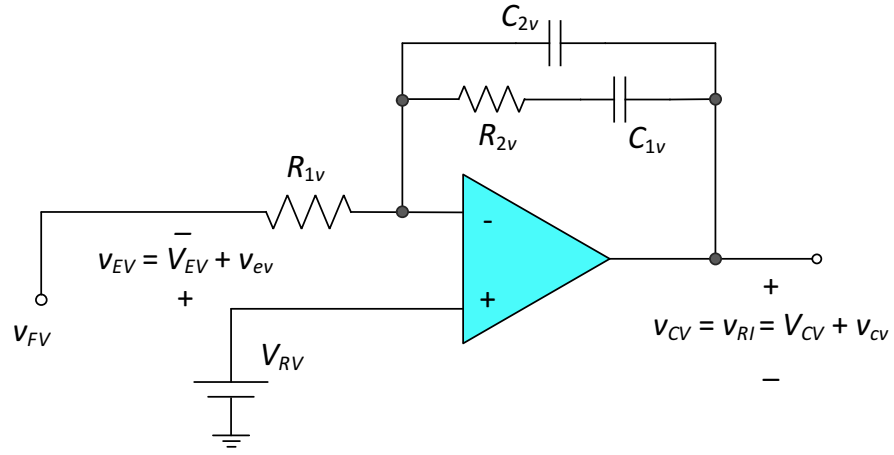

Figure 4.48: Circuit of type-II compensator used in outer-voltage loop.

where

$$T_{cvo} = \frac{1}{R_{1v}(C_{1v} + C_{2v})}, \tag{4.119}$$

$$\omega_{zcv} = \frac{1}{R_{2v}C_{1v}}, \tag{4.120}$$

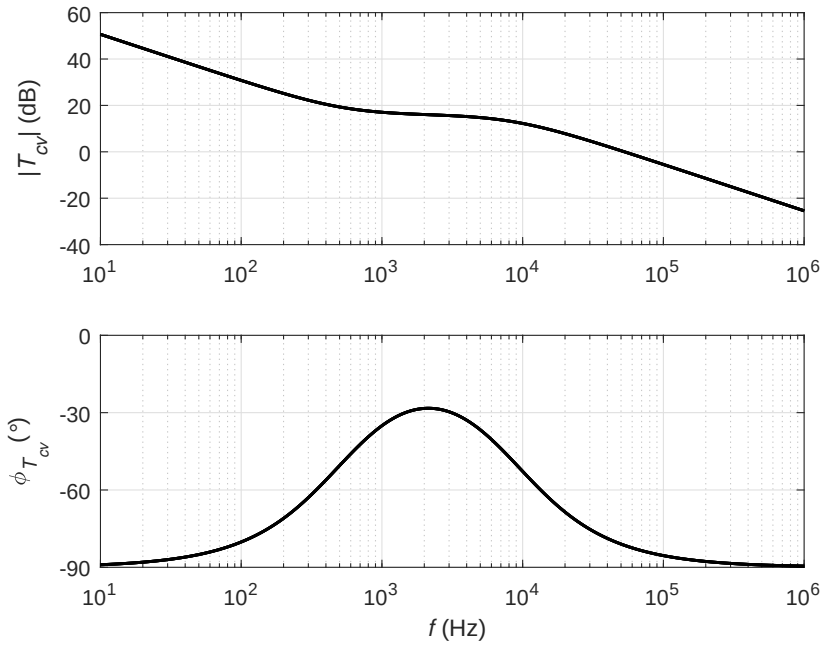

Figure 4.49: Theoretically obtained magnitude and phase plots of compensator transfer function T_{cv} for the outer-voltage loop.

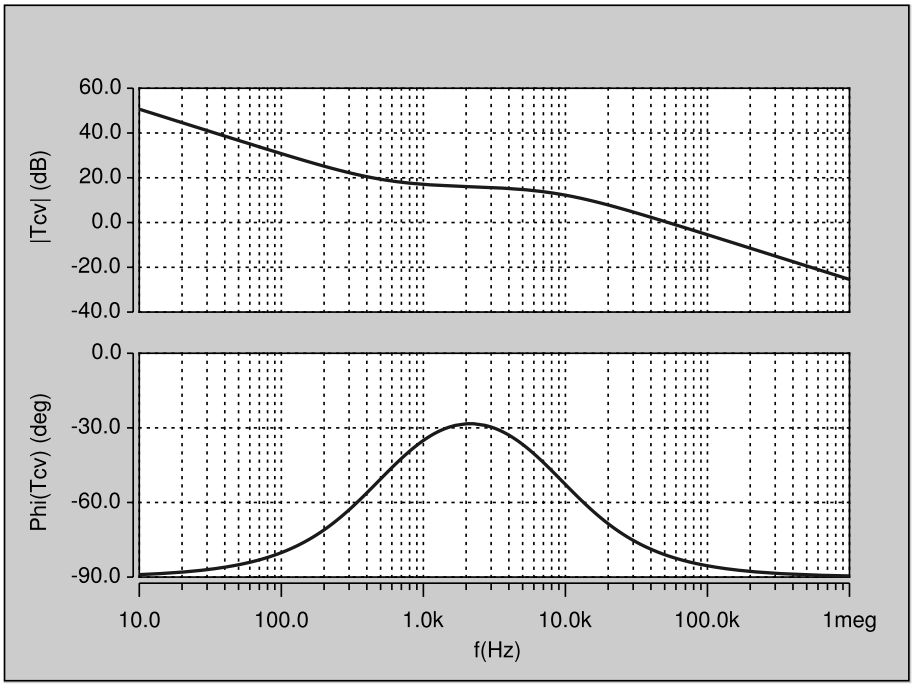

Figure 4.50: Magnitude and phase plots of the compensator transfer function T_{cv} for the outer-voltage loop obtained by circuit simulation.

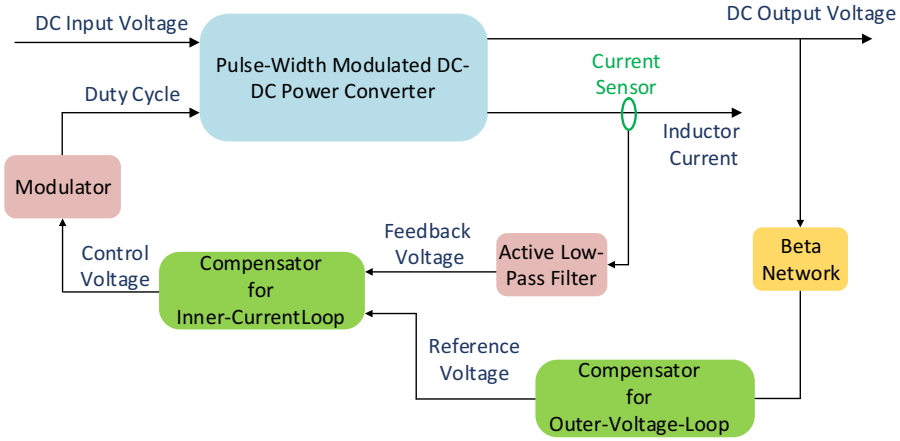

Figure 4.51: Architecture of true average current-mode control boost converter with outer-voltage loop.

and

$$\omega_{pcv} = \frac{C_{1v} + C_{2v}}{R_{2v} C_{1v} C_{2v}}. \tag{4.121}$$

Fig. 4.49 shows the theoretically obtained magnitude and phase plots of the compensator transfer function used in the outer-voltage loop. The theoretical results were validated by simulation. Fig. 4.50 shows the magnitude and phase plots of the compensator transfer function used in the outer-voltage loop using SABER Simulator.

4.7.3 Loop Gain of Outer-Voltage Loop T_v

The loop gain of the outer-voltage loop is

$$T_v = \frac{v_{ev}}{v_{fv}} = T_{kv} T_{cv} = \frac{\beta T_{ci} T_m T_p T_{cv}}{1 + T_i} = \frac{T_o}{1 + T_i}, \tag{4.122}$$

where $T_o = \beta T_{ci} T_m T_p T_{cv}$. Fig. 4.53 shows the theoretically obtained magnitude and phase plots of the loop gain of outer-voltage loop. The theoretical results were validated by simulation. Fig. 4.54 shows the magnitude and phase plots of the loop gain of outer-voltage loop using SABER Simulator.

4.8 Closed-Loop Transfer Functions for Outer-Voltage Loop

The following closed-loop control transfer functions are derived:

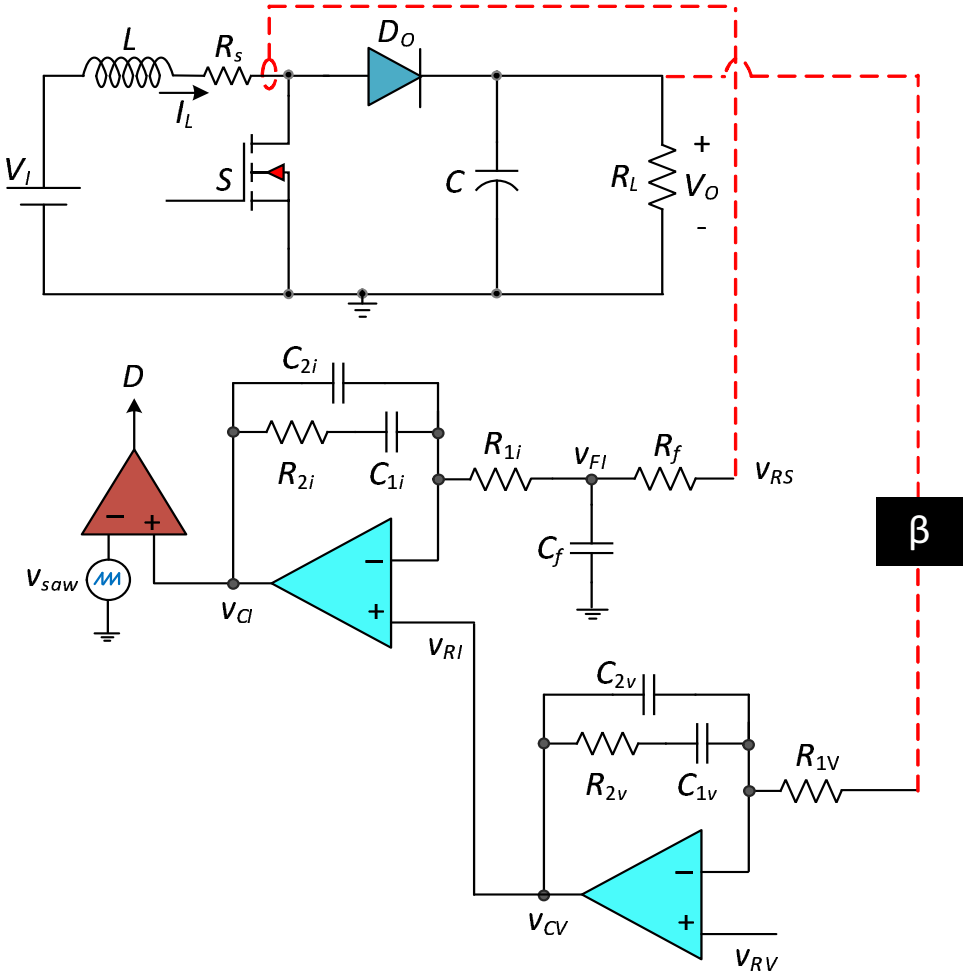

Figure 4.52: Circuit of average current-mode-control boost converter with outer-voltage loop.

- Reference voltage-to-output voltage transfer function T_{pcl}
- Input voltage-to-output voltage transfer function M_{vcl}
- Input voltage-to-duty-cycle transfer function M_{dv}
- Input impedance Z_{ivcl}
- Output impedance Z_{ovcl}

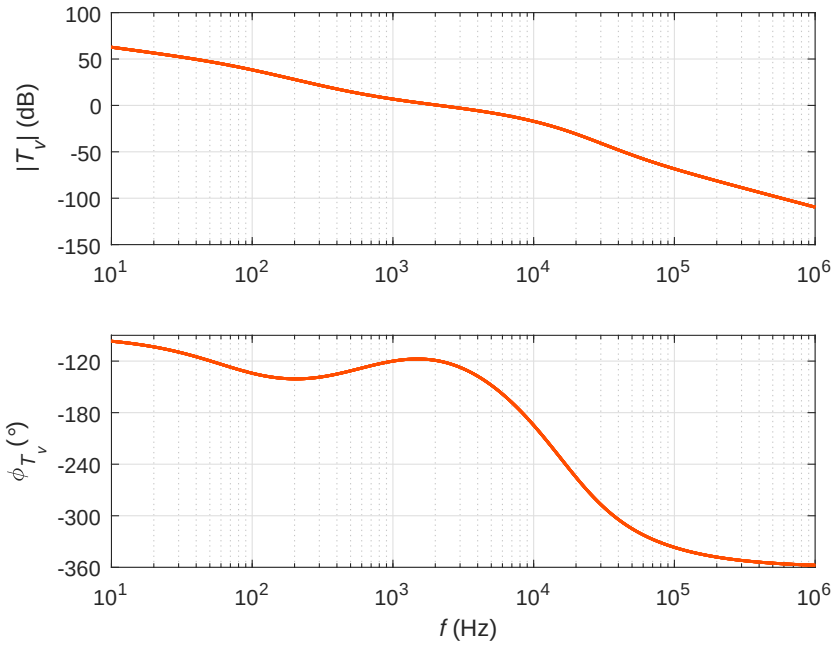

Figure 4.53: Theoretically obtained magnitude and phase plots of the loop gain T_v of the compensated outer-voltage loop.

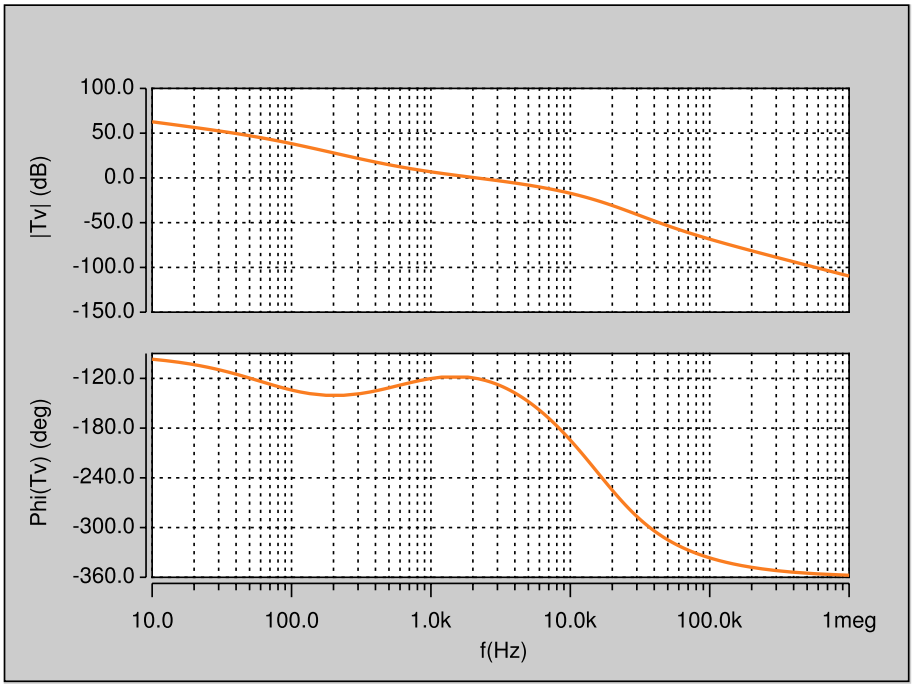

Figure 4.54: Magnitude and phase plots of the loop gain T_v of the compensated outer-voltage loop obtained by circuit simulation.

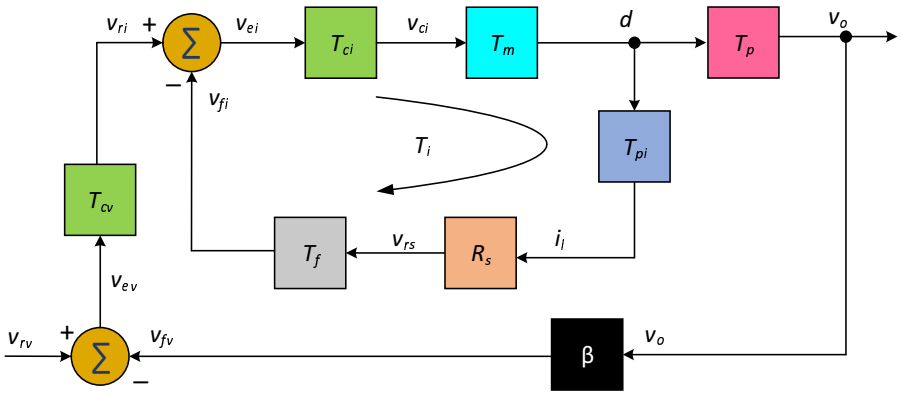

Figure 4.55: Block diagram used to derive control-to-output voltage transfer function T_{pcl}.

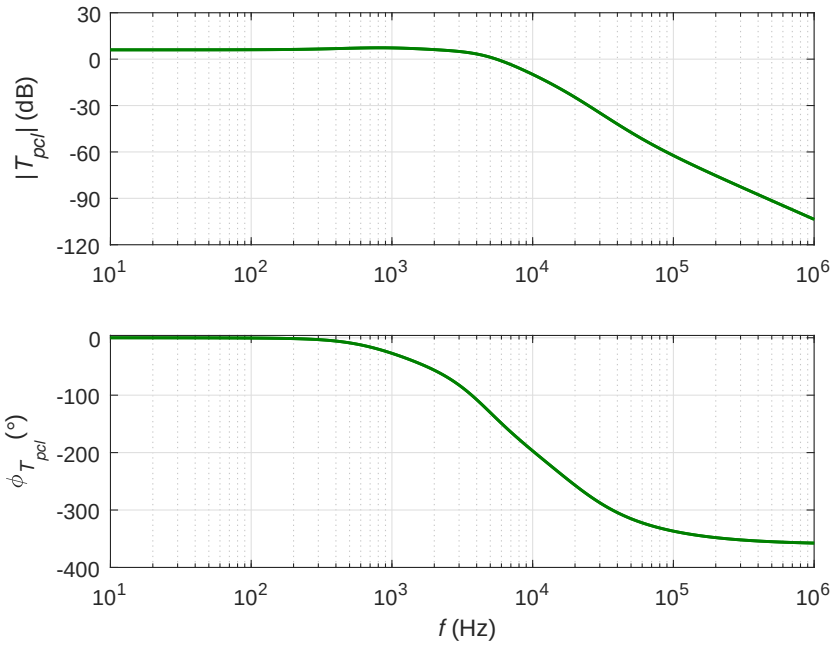

Figure 4.56: Theoretically obtained magnitude and phase plots of the reference voltage-to-output voltage transfer function T_{pcl}.

4.8.1 Reference Voltage-to-Output Voltage Transfer Function T_{pcl}

Using the block diagram shown in Fig. 4.55, the closed-loop reference voltage-to-output voltage transfer function is

$$T_{pcl}(s) = \frac{v_o(s)}{v_{rv}(s)} = \frac{T_{cv}T_{picl}}{1+T_v}. \tag{4.123}$$

Fig. 4.56 shows the theoretically obtained magnitude and phase plots of the reference voltage-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 4.57 shows the magnitude and phase plots of the reference voltage-to-output voltage transfer function using SABER Simulator.

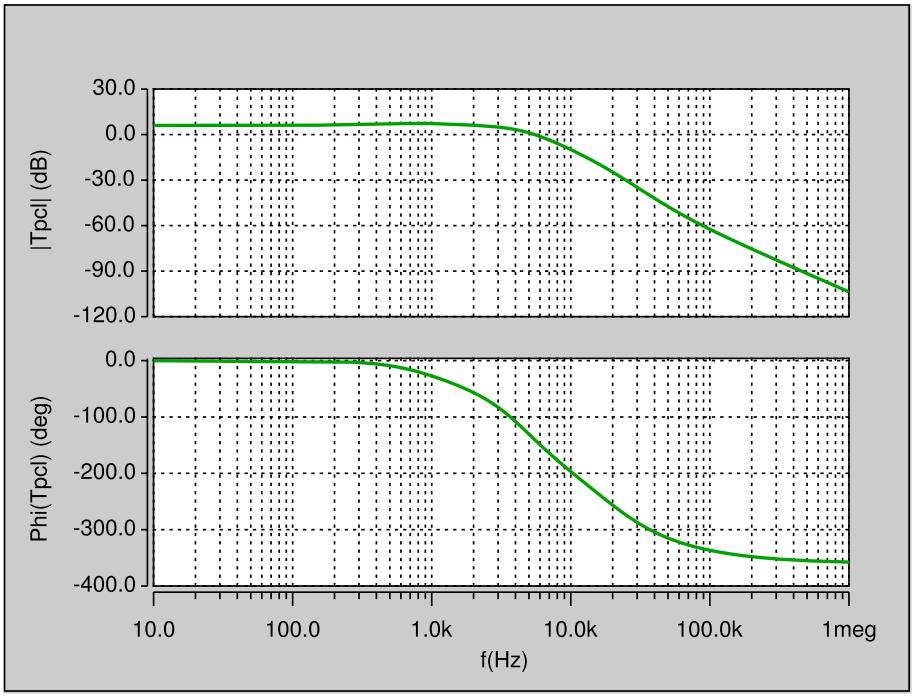

Figure 4.57: Magnitude and phase plots of the reference voltage-to-output voltage transfer function T_{pcl} obtained by circuit simulation.

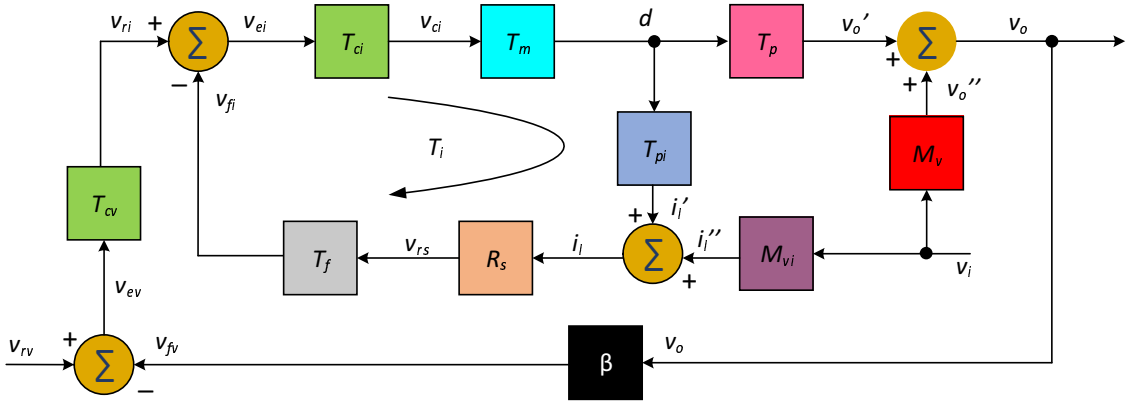

Figure 4.58: Block diagram used to derive the input voltage to duty-cycle transfer function M_{dv}.

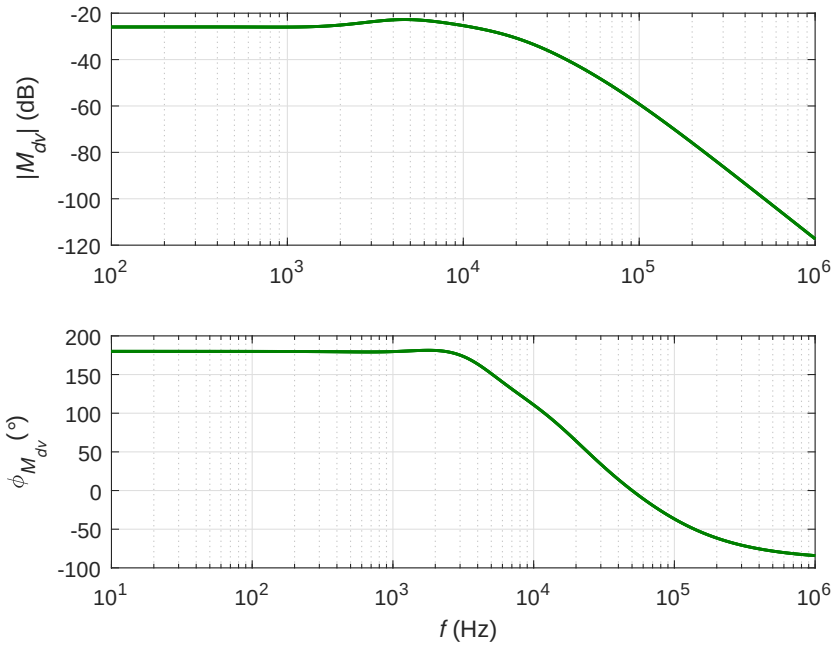

Figure 4.59: Theoretically obtained magnitude and phase plots of the input voltage-to-duty cycle transfer function M_{dv}.

4.8.2 Input Voltage to Duty-Cycle Transfer Function M_{dv}

Using the block diagram shown in Fig. 4.58, the closed-loop input voltage to duty-cycle transfer function is

$$M_{dv}(s) = \frac{d(s)}{v_i(s)} \tag{4.124}$$

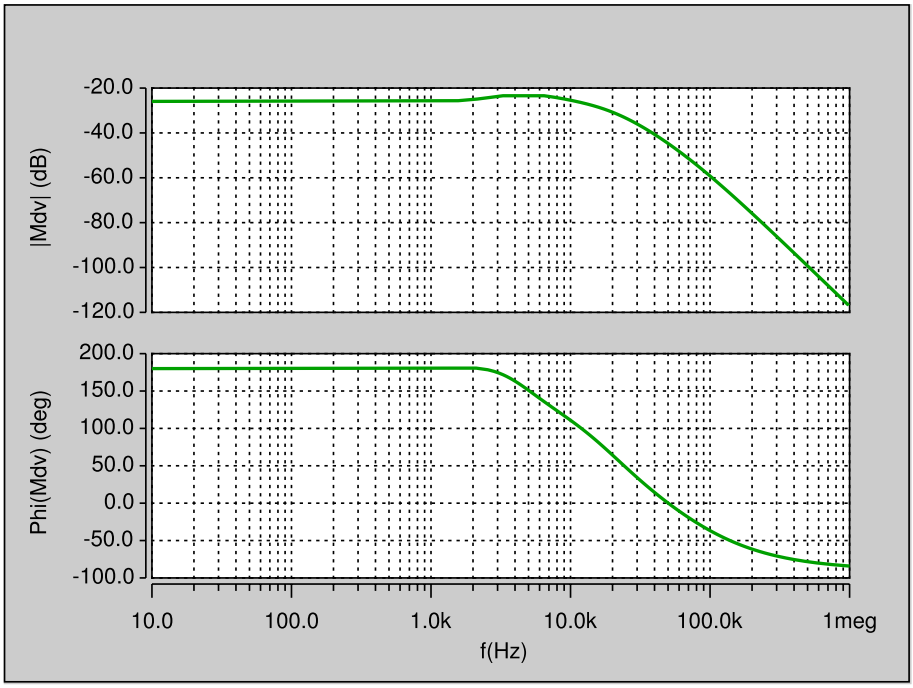

Figure 4.60: Magnitude and phase plots of the loop gain of the the input voltage-to-duty cycle transfer function M_{dv} obtained by circuit simulation.

From the block diagram

$$v_o = v_o' + v_o'' = T_p d + M_v v_i. \tag{4.125}$$

Also

$$v_{fv} = -\beta v_o \tag{4.126}$$

and

$$v_{cv} = v_{ri} = -\beta T_{cv} v_o. \tag{4.127}$$

The error voltage v_{ei} is

$$v_{ei} = v_{ri} - v_{fi} = -T_{cv}\beta v_o - R_s T_f i_l. \tag{4.128}$$

also

$$v_{ei} = \frac{d}{T_m T_{ci}}. \tag{4.129}$$

The inductor current is

$$i_l = T_{pi} d + M_{vi} v_i \tag{4.130}$$

Substituting (4.130) and (4.129) in (4.128), yields

$$\frac{d}{T_m T_{ci}} = -T_{cv}\beta v_o - R_s T_f (T_{pi} d + M_{vi} v_i). \tag{4.131}$$

Rearranging

$$v_o = -\frac{d}{T_{cv}\beta}\left(\frac{1}{T_m T_{ci}} + R_s T_f T_{pi}\right) - \frac{v_i}{T_{cv}\beta}\left(R_s T_f M_{vi}\right), \tag{4.132}$$

Equating (4.125) and (4.132) and rearranging

$$v_i\left(-\frac{M_{vi} R_s T_f}{T_{cv}\beta} - M_v\right) = d\left(T_p + \frac{1}{T_m T_{ci} T_{cv}\beta} + \frac{R_s T_f T_{pi}}{T_{cv}\beta}\right) \tag{4.133}$$

Equating (4.125) and (4.132) and rearranging

$$-\frac{v_i}{T_{cv}\beta}\left(M_{vi} R_s T_f + M_v T_{cv}\beta\right) = \frac{d}{T_{cv}\beta}\left(T_p T_{cv}\beta + \frac{1 + R_s T_f T_{pi} T_m T_{ci}}{T_m T_{ci}}\right). \tag{4.134}$$

Rearranging further

$$-v_i\left(M_{vi} R_s T_f + M_v T_{cv}\beta\right) = d\left(T_p T_{cv}\beta + \frac{1 + R_s T_f T_{pi} T_m T_{ci}}{T_m T_{ci}}\right) \tag{4.135}$$

and

$$M_{dv}(s) = \frac{d(s)}{v_i(s)} = -\frac{M_{vi} R_s T_f + \beta M_v T_{cv}}{\beta T_p T_{cv} + \dfrac{1 + T_i}{T_m T_{ci}}} \tag{4.136}$$

Fig. 4.59 shows the theoretically obtained magnitude and phase plots of the input voltage-to-duty cycle transfer function. The theoretical results were validated by simulation. Fig. 4.60 shows the magnitude and phase plots of the input voltage-to-duty cycle transfer function using SABER Simulator.

4.8.3 Input Voltage to Output Voltage Transfer Function M_{vcl}

Using the block diagram shown in Fig. 4.61, the closed-loop input voltage to output voltage transfer function with outer-voltage-loop is

$$M_{vcl}(s) = \frac{v_o(s)}{v_i(s)}. \tag{4.137}$$

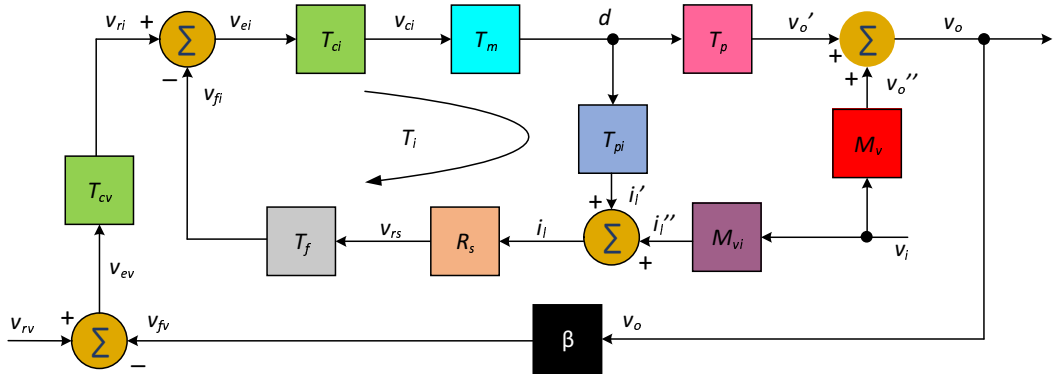

Figure 4.61: Block diagram used to derive the input voltage-to-output voltage transfer function M_{vcl}.

From (4.124)

$$d(s) = M_{dv} v_i(s). \tag{4.138}$$

Substituting (4.138) in

$$v_o = v_o' + v_o'' = T_p d + M_v v_i = T_p M_{dv} v_i + M_v v_i. \tag{4.139}$$

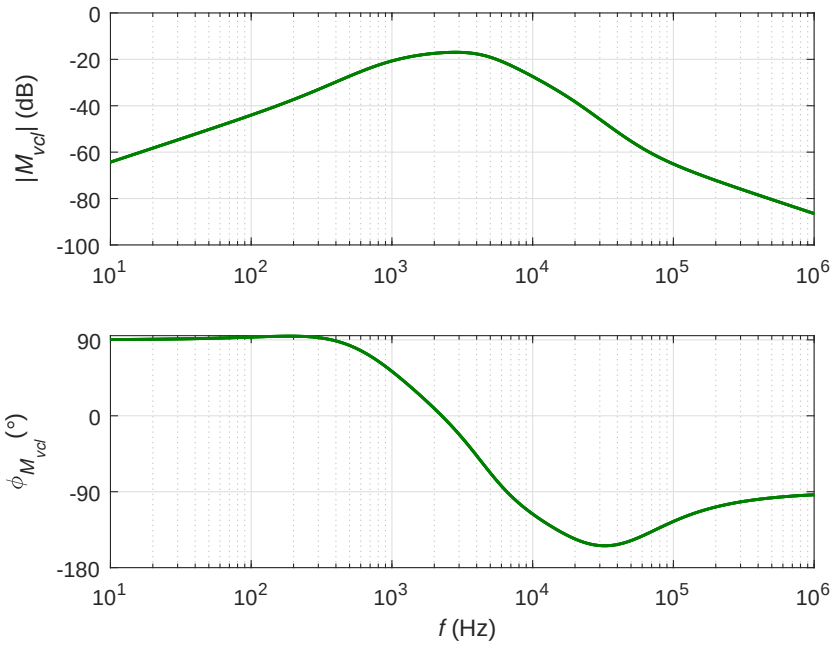

Figure 4.62: Theoretically obtained magnitude and phase plots of the input voltage-to-output voltage transfer function M_{vcl}.

Rearrangement of (4.139) yeilds

$$M_{vcl}(s) = \frac{v_o(s)}{v_i(s)} = T_p M_{dv} + M_v. \tag{4.140}$$

Fig. 4.62 shows the theoretically obtained magnitude and phase plots of the input voltage-to-output voltage transfer function M_{vcl}. The theoretical results were validated by simulation. Fig. 4.63 shows the magnitude and phase plots of the input voltage-to-output voltage transfer function M_{vcl} using SABER Simulator.

4.8.4 Input Impedance Z_{ivcl}

Using the block diagram shown in Fig. 4.64, the closed-loop input impedance with outer-voltage-loop is

$$Z_{ivcl}(s) = \frac{v_i(s)}{i_i(s)}. \tag{4.141}$$

From the Fig. 4.64,

$$v_o = v_o' + v_o'' = T_p d + M_v v_i \tag{4.142}$$

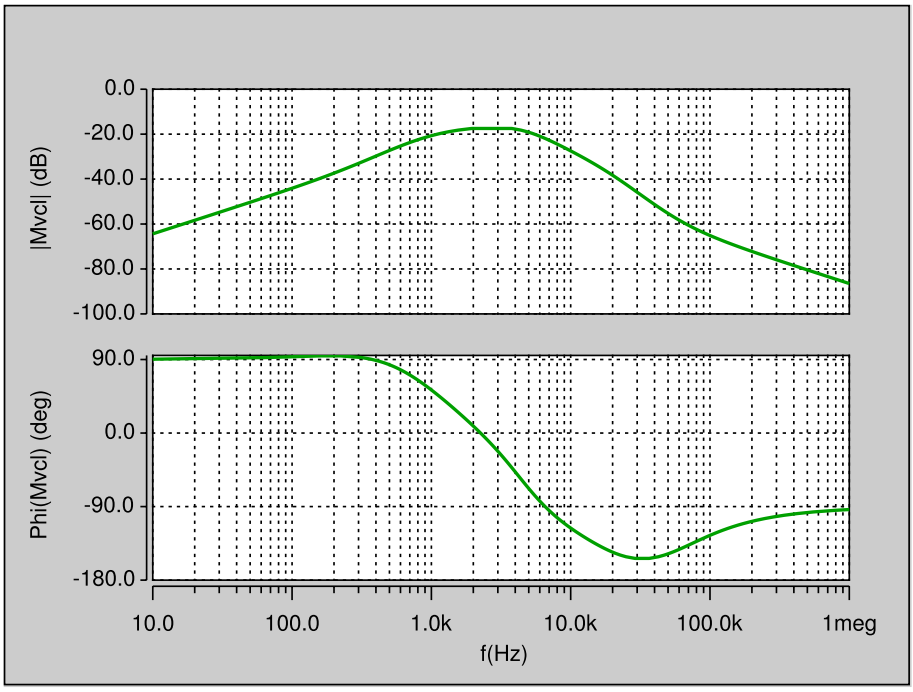

Figure 4.63: Magnitude and phase plots of the loop gain the input voltage-to-output voltage transfer function M_{vcl} obtained by circuit simulation.

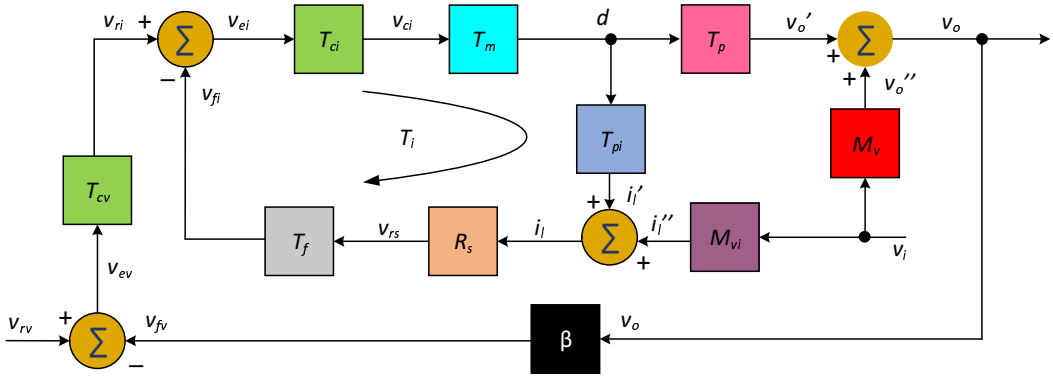

Figure 4.64: Block diagram used to derive the closed outer-voltage loop input impedance Z_{ivcl}.

and

$$i_i = i_l = i_l' + i_l'' = T_{pi}d + M_{vi}v_i. \tag{4.143}$$

Also

$$v_{fv} = \beta v_o, \tag{4.144}$$

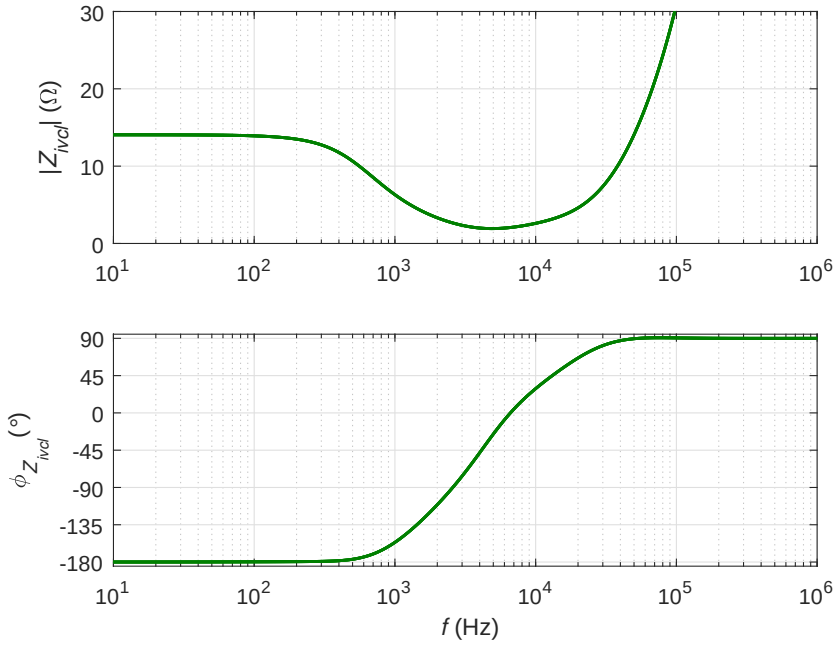

Figure 4.65: Theoretically obtained magnitude and phase plots of the closed outer-voltage loop input impedance Z_{ivcl}.

$$v_{ev} = v_{rv} - v_{fv} = 0 - \beta v_o = -\beta v_o \tag{4.145}$$

and

$$v_{cv} = v_{ri} = T_{cv} v_{ev} = -\beta T_{cv} v_o. \tag{4.146}$$

The error voltage v_{ei} is

$$v_{ei} = \frac{d}{T_{ci} T_m}. \tag{4.147}$$

The feedback voltage v_{fi} is

$$v_{fi} = T_f R_s i_l. \tag{4.148}$$

The reference voltage to inner-current-loop is

$$v_{ri} = v_{ei} + v_{fi}. \tag{4.149}$$

Substituting (4.146), (4.147) and (4.148) in (4.149)

$$-\beta T_{cv} v_o = \frac{d}{T_{ci} T_m} + T_f R_s i_l. \tag{4.150}$$

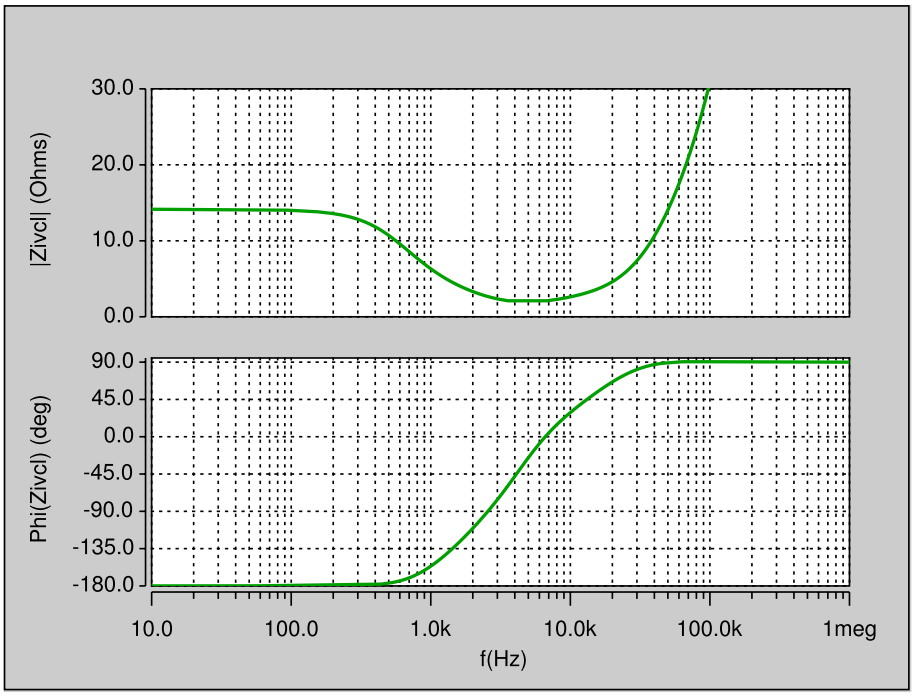

Figure 4.66: Magnitude and phase plots of the closed outer-voltage loop input impedance Z_{ivcl} obtained by circuit simulation.

Rearranging

$$v_o = -\frac{d}{\beta T_{cv} T_{ci} T_m} - \frac{T_f R_s i_l}{\beta T_{cv}}. \tag{4.151}$$

Substituting (4.142) in (4.151)

$$T_p d + M_v v_i = -\frac{d}{\beta T_{cv} T_{ci} T_m} - \frac{T_f R_s i_l}{\beta T_{cv}}. \tag{4.152}$$

Rearranging

$$d\left(T_p + \frac{1}{\beta T_{cv} T_{ci} T_m}\right) = -\frac{T_f R_s i_l}{\beta T_{cv}} - M_v v_i. \tag{4.153}$$

substituting (4.143) in (4.153)

$$d\left(T_p + \frac{1}{\beta T_{cv} T_{ci} T_m}\right) = -\frac{T_f R_s (T_{pi} d + M_{vi} v_i)}{\beta T_{cv}} - M_v v_i. \tag{4.154}$$

$$d\left(T_p + \frac{1}{\beta T_{cv} T_{ci} T_m} + \frac{T_f R_s T_{pi}}{\beta T_{cv}}\right) = \left(-\frac{T_f R_s M_{vi}}{\beta T_{cv}} - M_v\right). \tag{4.155}$$

$$d\left(\frac{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m}{\beta T_{ci} T_m T_{cv}}\right) = \left(\frac{-T_f R_s M_{vi} - \beta T_{cv} M_v}{\beta T_{cv}}\right). \tag{4.156}$$

$$d = -\frac{T_{ci} T_m (T_f R_s M_{vi} + \beta M_v T_{cv})}{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m} v_i \tag{4.157}$$

Substituting (4.157) in (4.143)

$$i_i = \left[-\frac{T_{ci} T_m (T_f R_s M_{vi} + \beta M_v T_{cv})}{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m} T_{pi} + M_{vi} \right] v_i \tag{4.158}$$

The closed-loop input admittance with outer-voltage-loop is

$$Y_{ivcl}(s) = \frac{i_i(s)}{v_i(s)} = -\frac{T_{ci} T_m (T_f R_s M_{vi} + \beta M_v T_{cv})}{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m} T_{pi} + M_{vi} \tag{4.159}$$

The closed-loop input impedance with outer-voltage-loop is

$$Z_{ivcl}(s) = \frac{v_i(s)}{i_i(s)} = \frac{1}{Y_{ivcl}(s)}. \tag{4.160}$$

Fig. 4.65 shows the theoretically obtained magnitude and phase plots of the closed-loop input impedance Z_{ivcl}. The theoretical results were validated by simulation. Fig. 4.66 shows the magnitude and phase plots of the closed-loop input impedance Z_{ivcl} using SABER Simulator.

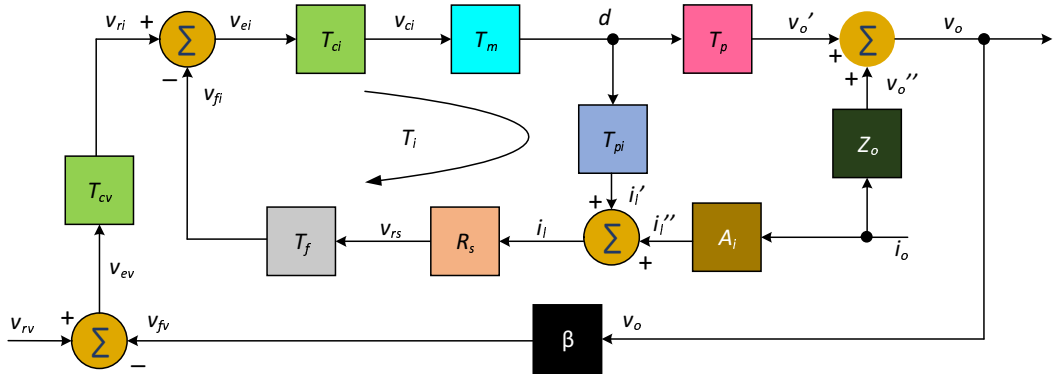

Figure 4.67: Block diagram used to derive the closed outer-voltage loop output impedance Z_{ovcl}.

4.8.5 Output Impedance Z_{ovcl}

Using the block diagram shown in Fig. 4.67, the closed-loop output impedance with outer-voltage-loop is

$$Z_{ovcl}(s) = \frac{v_o(s)}{i_o(s)}. \tag{4.161}$$

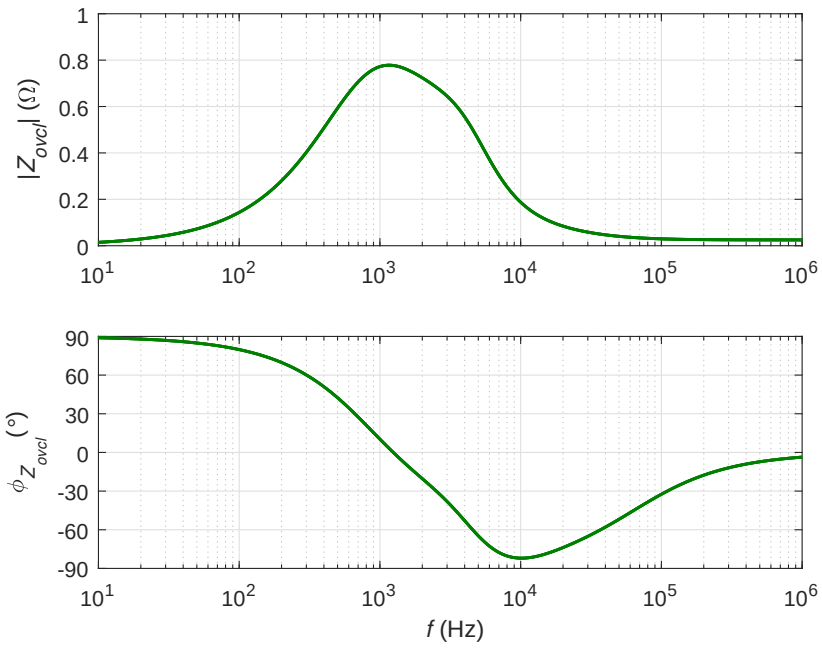

Figure 4.68: Theoretically obtained magnitude and phase plots of the closed outer-voltage loop output impedance Z_{ovcl}.

From the Fig. 4.67,

$$v_o = v_o' + v_o'' = T_p d + Z_o i_o. \tag{4.162}$$

and

$$i_l = i_l' + i_l'' = A_i i_o + T_{pi} d. \tag{4.163}$$

Also

$$v_{fv} = \beta v_o \tag{4.164}$$

and

$$v_{cv} = v_{ri} = -\beta T_{cv} v_o. \tag{4.165}$$

The error voltage v_{ei} is

$$v_{ei} = v_{ri} - v_{fi} = -T_{cv}\beta v_o - R_s T_f i_l. \tag{4.166}$$

and

$$v_{ei} = \frac{d}{T_m T_{ci}}. \tag{4.167}$$

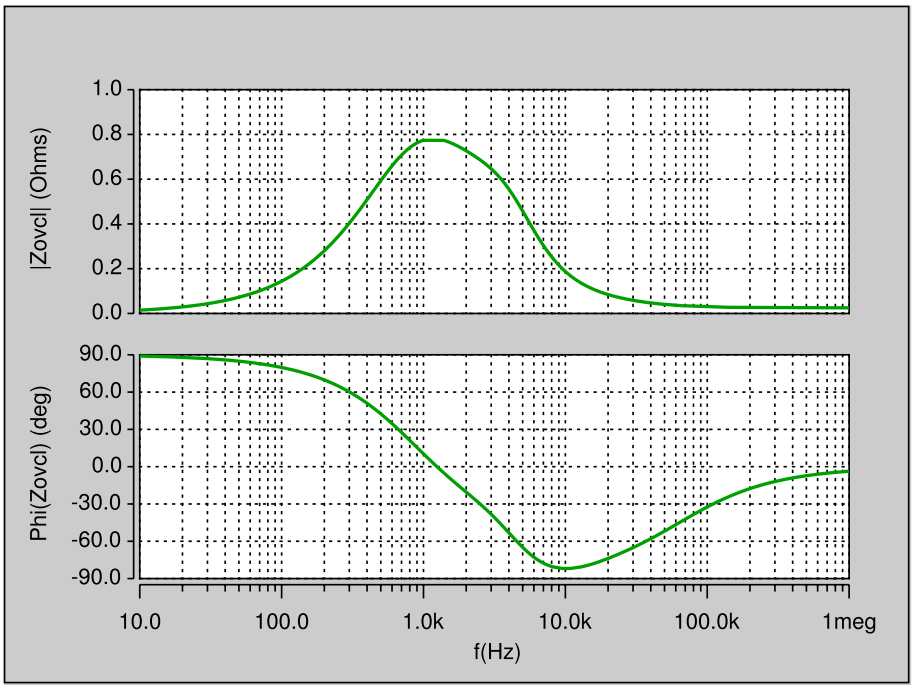

Figure 4.69: Magnitude and phase plots of the closed outer-voltage loop output impedance Z_{ovcl} obtained by circuit simulation.

Substituting (4.163) and (4.167) in (4.166), yields

$$\frac{d}{T_m T_{ci}} = -T_{cv}\beta v_o - R_s T_f (A_i i_o + T_{pi} d.). \tag{4.168}$$

Rearranging (4.168)

$$d = -\frac{(T_{cv}\beta v_o + R_s T_f A_i i_o) T_{ci} T_m}{1 + T_i} \tag{4.169}$$

Substituting (4.169) in (4.162), yields

$$v_o = T_p \left[- \frac{(T_{cv}\beta v_o + R_s T_f A_i i_o) T_{ci} T_m}{1 + T_i} \right] + Z_o i_o. \tag{4.170}$$

Rearranging

$$v_o \left(1 + \frac{\beta T_p T_{cv} T_{ci} T_m}{1 + T_i} \right) = i_o \left(Z_o - \frac{T_p R_s T_f A_i T_{ci} T_m}{1 + T_i} \right) \tag{4.171}$$

Hence the closed-loop output impedance with outer-voltage-loop is

$$Z_{ovcl}(s) = \frac{v_o(s)}{i_o(s)} = \frac{Z_o(1 + T_i) - A_i T_p T_{ix}}{1 + T_i + T_p T_{cv} \beta T_{ci} T_m} = \frac{Z_o(1 + T_i) - A_i T_p T_{ix}}{1 + T_i + T_o}. \tag{4.172}$$

Fig. 4.68 shows the theoretically obtained magnitude and phase plots of the closed-loop output impedance Z_{ovcl}. The theoretical results were validated by simulation. Fig. 4.69 shows the magnitude and phase plots of the closed-loop output impedance Z_{ovcl} using SABER Simulator.

4.9 Results

The key results of the small-signal analysis, step responses of open-loop, and closed-loop transfer functions are discussed in this section. The pole-zero plots are also presented to illustrate the relocation of the power stage poles and zeros with the introduction of inner-current and outer-voltage loops.

Fig. 4.70 shows a comparison of the responses in output voltage of the boost converter for a step change in the duty cycle by 0.1 unit for T_p and a step change in the reference voltage by 1 V in T_{picl} and T_{pcl}. A change in duty cycle by 0.1 unit

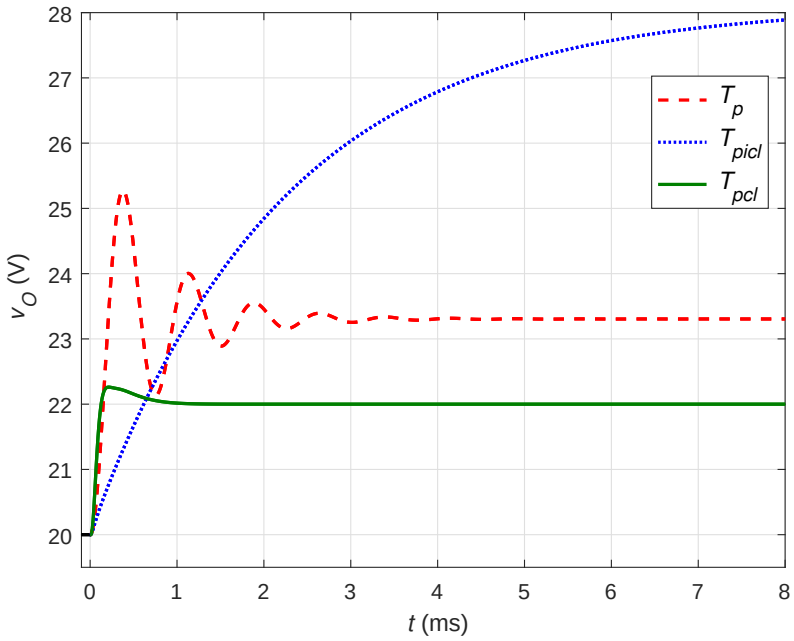

Figure 4.70: Comparison of responses in output voltages for step changes in duty cycle, current-loop reference, and voltage-loop reference voltages obtained using T_p, T_{picl}, and T_{pcl} transfer functions, respectively.

corresponds to a change in the output voltage by nearly 3.3055 V. A similar steady-state response can be observed for the T_{picl} transfer function, however, the response is slower than open-loop response. With the outer-voltage loop closed, an improved response to step change in the reference voltage can be observed. The output voltage changes by nearly 2 V and exhibits a short rise time and settling time characteristics. In conclusion, the response to output voltage is improved in the presence of a current-controlled power stage.

Fig. 4.71 shows a comparison of the responses in output voltage for a step change in the input voltage by 1 V in the power stage, current-controlled power stage, and closed-outer loop. The input-to-output voltage transfer functions M_v, M_{vicl}, and M_{vcl} corresponding to the boost power stage, power stage with only inner loop control, and boost with both inner and outer loops are shown. The open-loop converter is highly susceptible to change in the input voltage. For example, for a 1 V change in the input

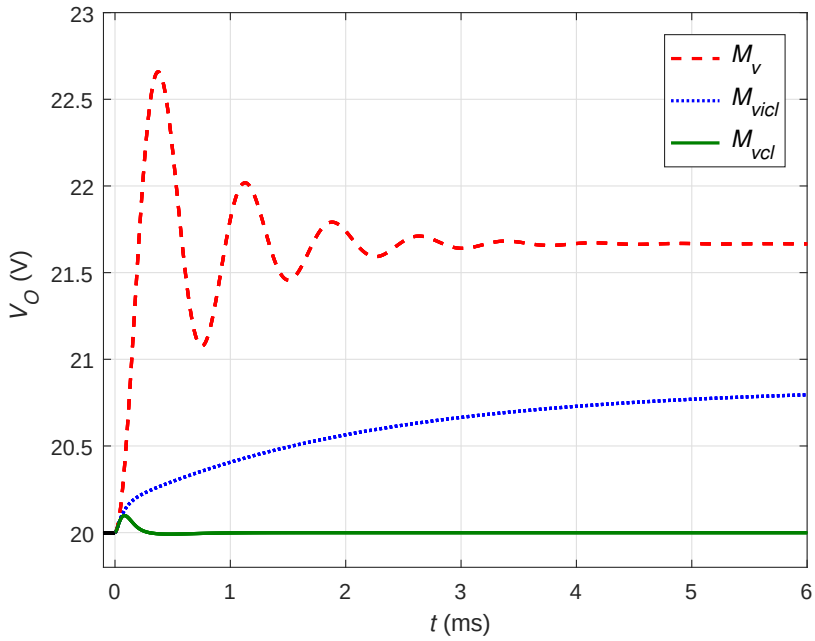

Figure 4.71: Comparison of responses in output voltages for step changes in input voltage by 1 V obtained using M_v, M_{vicl}, and M_{vcl} transfer functions, respectively.

voltage, the output voltage in an open-loop converter changes by nearly 1.6664 V. However, for a 1 V change in the input voltage, the output voltage of the converter with only the inner loop increases only by nearly 0.8 V. The inner current loop alone is not capable of providing 100% correction to changes in the input voltage. With the inclusion of the outer-voltage loop, the audio-susceptibility is further reduced significantly, where the output voltage is nearly unaffected by any change in the input voltage. Therefore, a two-loop control is the most suited topology for regulated power supplies.

Fig. 4.72 shows the comparison of the responses in input current for step change in the input voltage for the open-loop, power stage with only closed-inner loop, and with two-loop controlled boost dc-dc converter. In the dc-dc converter in open-loop configuration, the input current increases with increment in the input voltage. Therefore, the input impedance of an open-loop dc-dc converter offers a positive resistance

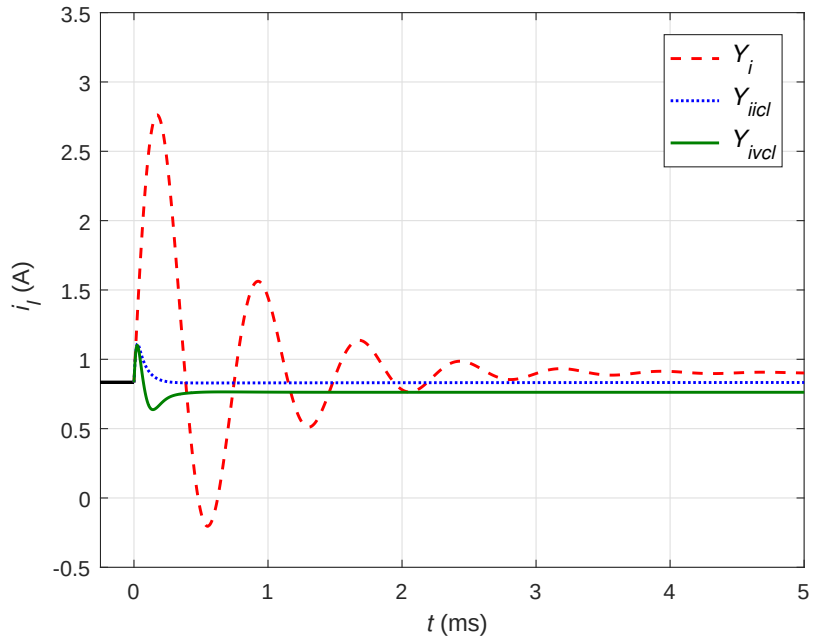

Figure 4.72: Comparison of the responses in input current for step change in the input voltage for the open-loop, power stage with only closed-inner loop, and with two-loop controlled boost dc-dc converter.

effect at dc in accordance with Ohm's law.

Fig. 4.73 shows the comparison of responses in the output voltage for step change in the load current by 1 A for the open-loop, power stage with only closed-inner loop, and with two-loop controlled boost dc-dc converter. In this analysis, it is assumed that a current source is placed across the load resistance, which injects current at the converter output node. In the open-loop dc-dc converter, the magnitude of the output voltage increases with increase in the magnitude of the current. Implementation of inner-current loop increases the magnitude of output resistance.

Fig. 4.74 shows the trajectory of the poles and zeros of the duty cycle-to-output voltage transfer function T_p obtained at selected values of the duty cycle D. The zero z_n caused by the filter capacitor C and its equivalent series resistance r_C do not move with the duty cycle as it is independent of the duty cycle. The location of the poles p_1, p_2 is severely affected by the duty cycle. A clearer illustration of the movement

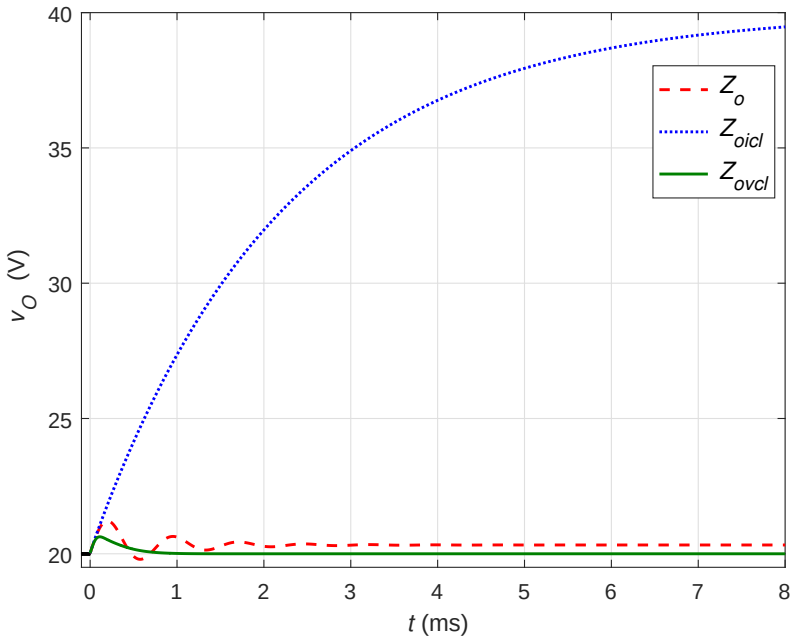

Figure 4.73: Comparison of responses in the output voltage for step changes in the load current by 1 A for the open-loop, power stage with only closed-inner loop, and with two-loop controlled boost dc-dc converter.

can be observed in Fig. 4.75. The RHP zero moves towards the origin with increase in the duty cycle. At low duty ratios, the zero is located in the right-half of the s-plane. With increase in the duty cycle, the RHP-zero moves towards the origin. At $R_L(1-D)^2 = r$, the RHP zero is at the origin. This corresponds to a critical duty cycle determined by

$$D_{cr} = 1 - \sqrt{\frac{r}{R_L}}. \tag{4.173}$$

Beyond $D > D_{cr}$, the RHP-zero shifts to the left-half of the s-plane.

The zero z_i is independent of the duty cycle. The poles p_1, p_2 are severely affected by the change in duty cycle. The location of the real component of the poles p_1, p_2 marginally moves towards $-\infty$. The imaginary component the poles p_1, p_2 reduces with increase in duty cycle. Beyond a critical duty cycle, the imaginary component of the poles meet the real axis and are transformed into real poles. The pole p_1 moves towards $-\infty$ while the pole p_2 moves towards the origin with increase in the duty

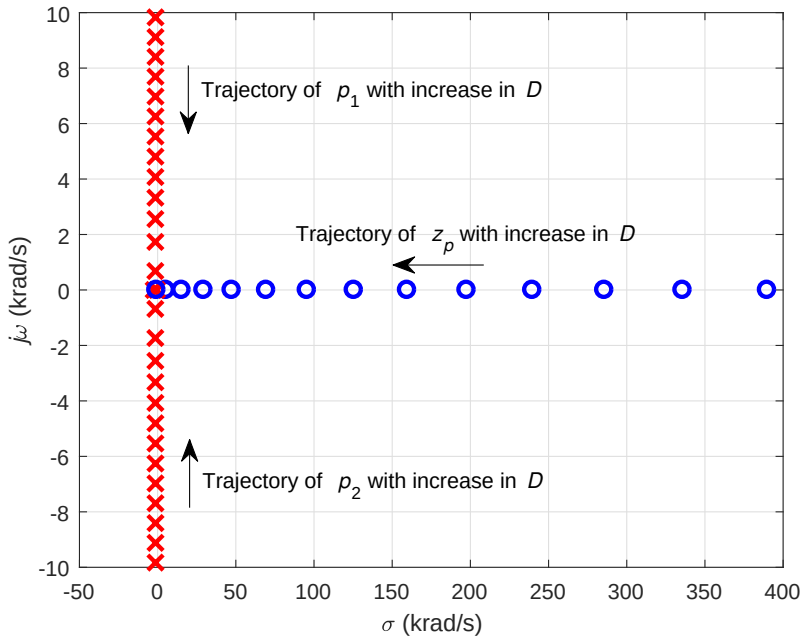

Figure 4.74: Trajectory of poles and zeros of the open-loop duty cycle-to-output voltage transfer function as functions of the duty cycle.

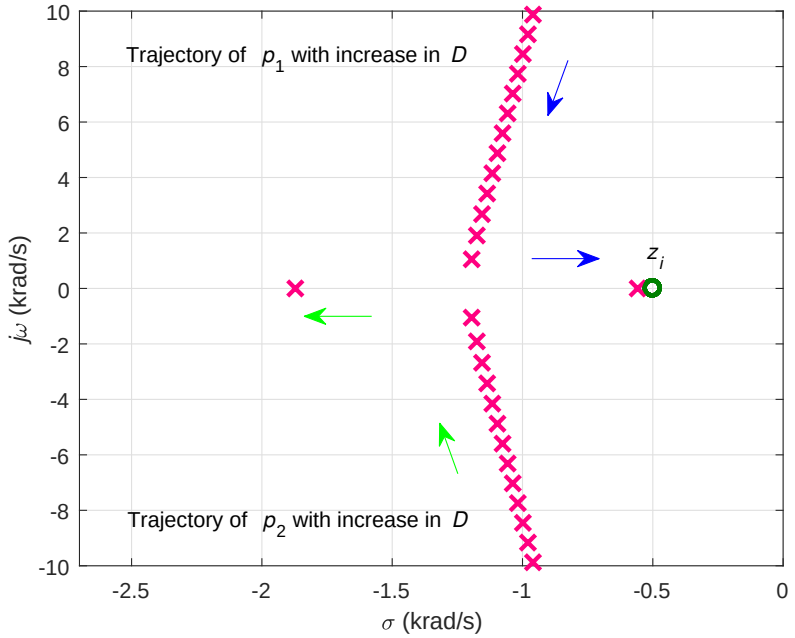

Figure 4.75: Trajectory of poles and zeros of the open-loop duty cycle-to-inductor current transfer function as functions of the duty cycle.

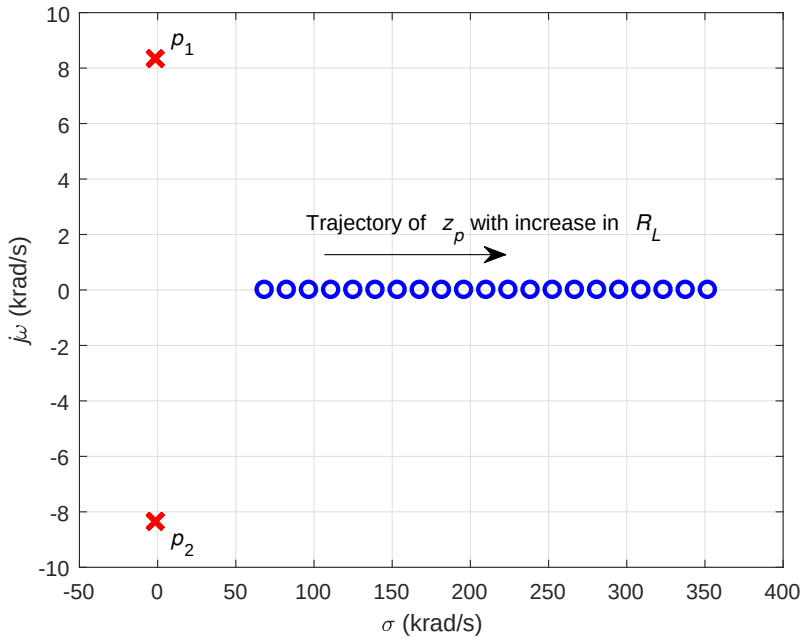

Figure 4.76: Trajectory of poles and zeros of the open-loop duty cycle-to-output voltage transfer function as functions of the load resistance.

cycle beyond a critical value.

Fig. 4.76 shows the trajectory of the poles and zeros of the duty cycle-to-output voltage transfer function T_p obtained at selected values of the load resistance R_L. The zero z_n caused by the filter capacitor C and its equivalent series resistance r_C do not move with the load resistance as it is independent of the load resistance. The location of the poles p_1, p_2 is not affected by the load resistance. A clearer illustration of the movement can be observed in Fig. 4.77. However, the RHP zero z_p moves towards ∞ with increase in the load resistance. This means that the converter stability is much larger at high load resistance or low output power. This plot indicates that the controller for the power-stage must be designed for the worst-case condition occurring at a minimum load resistance.

Fig. 4.77 shows the trajectory of the poles and zeros of the duty cycle-to-inductor current transfer function T_{pi} obtained at selected values of the load resistance R_L.

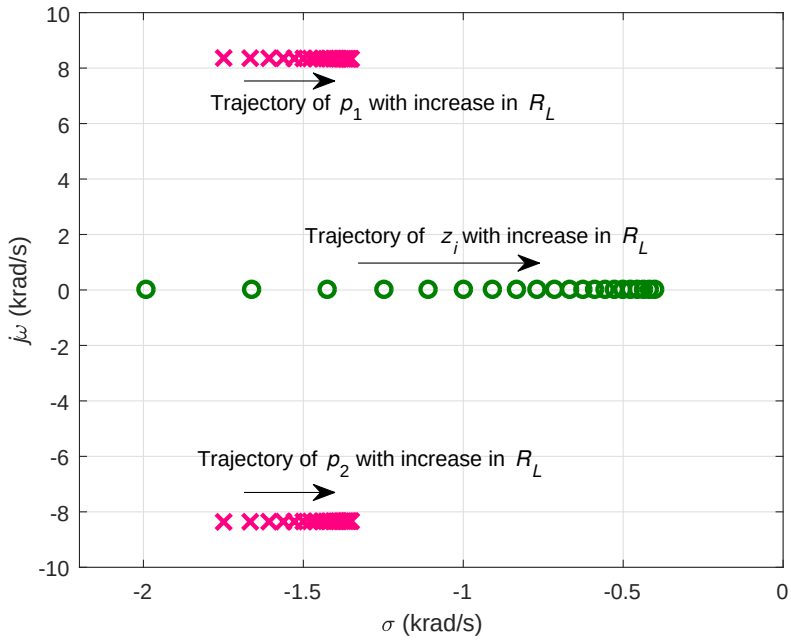

Figure 4.77: Trajectory of poles and zeros of the open-loop duty cycle-to-inductor current transfer function as functions of the load resistance.

One may clearly observe that the location of the poles p_1 and p_2 is not impacted by the variation in load resistance over the desired range. However, the low-frequency LHP zero z_i moves towards the origin with increase in load resistance. From the design point-of-view, the controller for the current loop must be designed for the maximum load resistance specifications or minimum output power.

Fig.4.78 shows the bode magnitude and phase plots of T_p at selected values of D. Fig.4.79 shows the bode magnitude and phase plots of T_{pi} at selected values of D. Fig. 4.80 shows the bode magnitude and phase plots of T_p at selected values of R_L. Fig. 4.81 shows the bode magnitude and phase plots of T_{pi} at selected values of R_L.

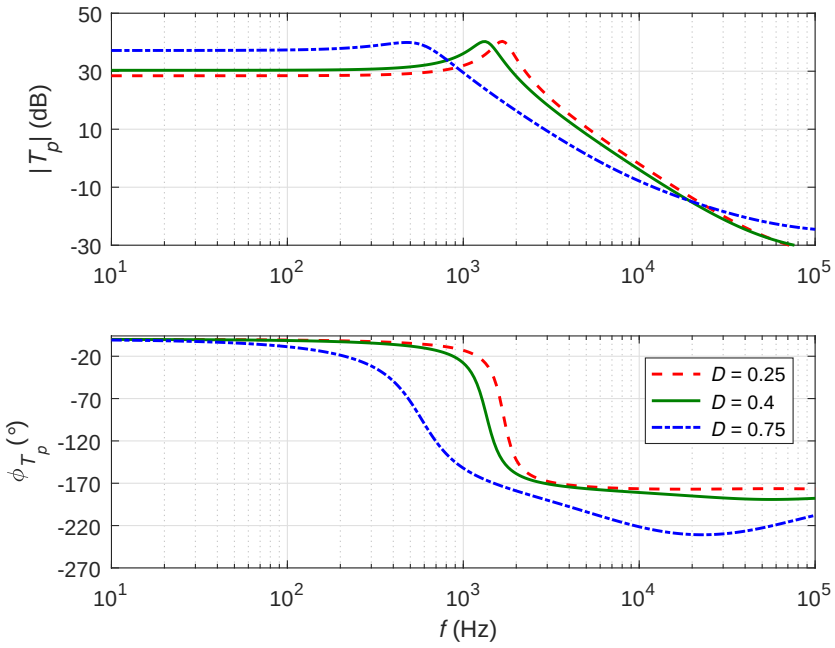

Figure 4.78: Bode magnitude and phase plots of T_p at selected values of D.

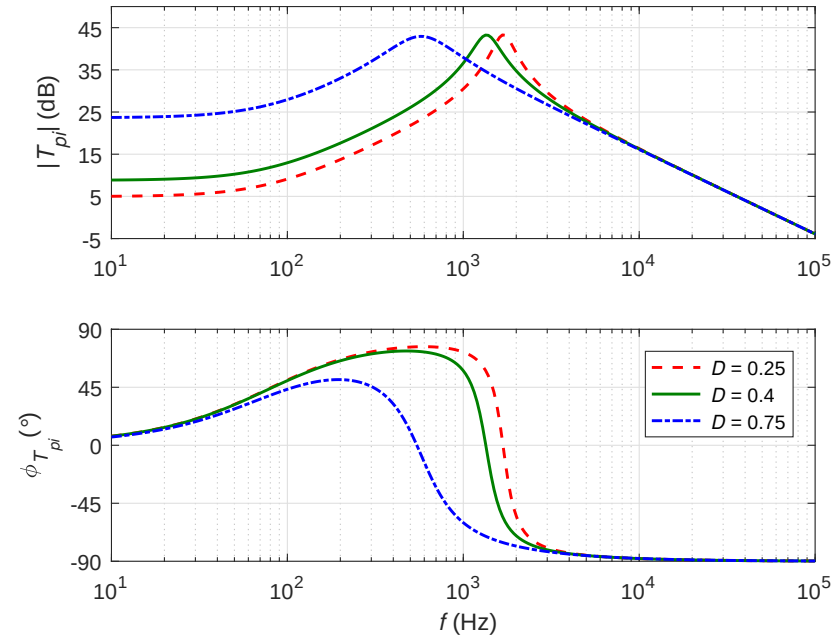

Figure 4.79: Bode magnitude and phase plots of T_{pi} at selected values of D.

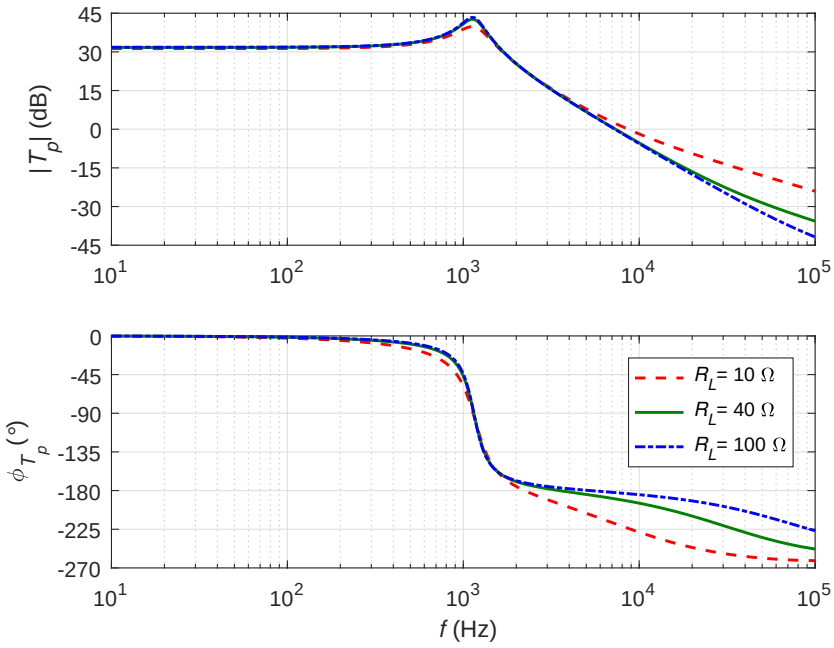

Figure 4.80: Bode magnitude and phase plots of T_p at selected values of R_L.

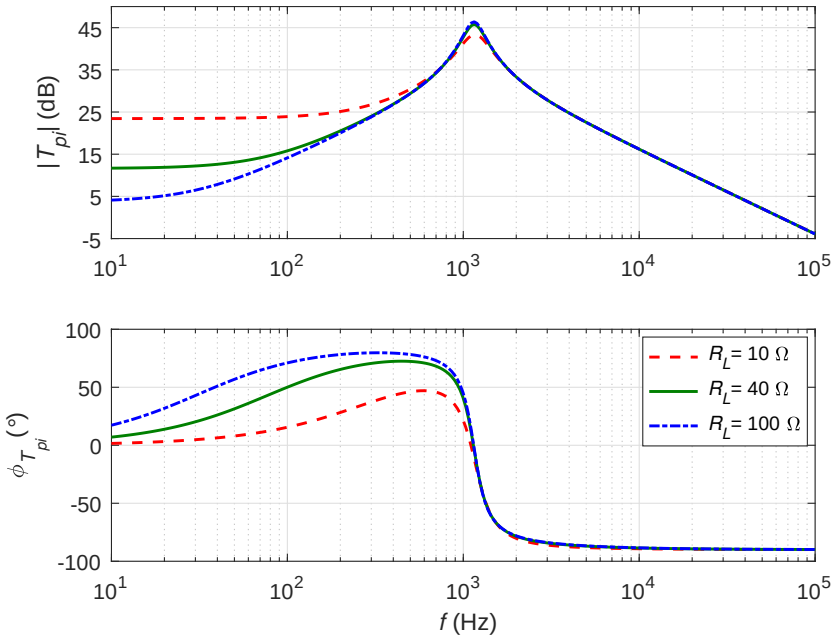

Figure 4.81: Bode magnitude and phase plots of T_{pi} at selected values of R_L.

5 True-Average Current-Mode-Control of Buck DC-DC Converter

The circuit of pulse-width modulated (PWM) buck converter is shown in Fig. 5.1. The operation of buck converter in continuous conduction mode (CCM) is given in details in [34]. The circuit of DC-DC buck converter consists of a power MOSFET S, a diode D_o, an inductor L, a filter capacitor C, and a load resistor R_L. The switch is turned on and off at a switching frequency f_s and at a duty cycle D. The converter efficiency is η. The aims of this chapter are

1. To describe the dc characteristics of buck dc-dc converter.
2. To develop the small-signal linear model of buck dc-dc converter.
3. To derive and analyze the open-loop power stage transfer functions of buck dc-dc converter.
4. To derive and analyze the open-loop input and output impedances of buck dc-dc converter.
5. To analyze and design a compensator circuit.
6. To demonstrate the behavior of true-average current-mode controlled (CMC) buck converter.
7. To derive and analyze the closed inner-current loop transfer functions.
8. To derive and analyze the closed outer-voltage loop transfer functions.

The analytical results such as magnitude and phase plots of transfer functions and step responses are described using MALATB. The theoretical predicted results are validated using circuit simulations performed on SABER by Synopsis.

5.1 DC Characteristics

The dc voltage transfer function of buck converter for CCM are given in details in [34]. The idealized current and voltage waveforms of the switching network of buck converter are shown in Fig. 5.2. Circuit averaging technique is applied to switching network waveforms. The dc component of the switch current is

$$I_S = \frac{1}{T}\int_0^T i_s dt = \frac{1}{DT}\int_0^T I_L dt = DI_L. \tag{5.1}$$

Hence, the MOSFET can be replaced by an ideal dc current-dependent current source. The dc component of diode voltage is

$$V_D = \frac{1}{T}\int_0^T v_d dt = \frac{1}{DT}\int_0^T V_I dt = DV_I. \tag{5.2}$$

The diode can be replaced by an ideal dc voltage-dependent voltage source. The dc component of the input current is

$$I_I = I_S = DI_L \tag{5.3}$$

and the dc component of output current is

$$I_O = I_L. \tag{5.4}$$

The dc voltage transfer function of the ideal converter is

$$M_{VDC} = \frac{V_O}{V_I} = D \tag{5.5}$$

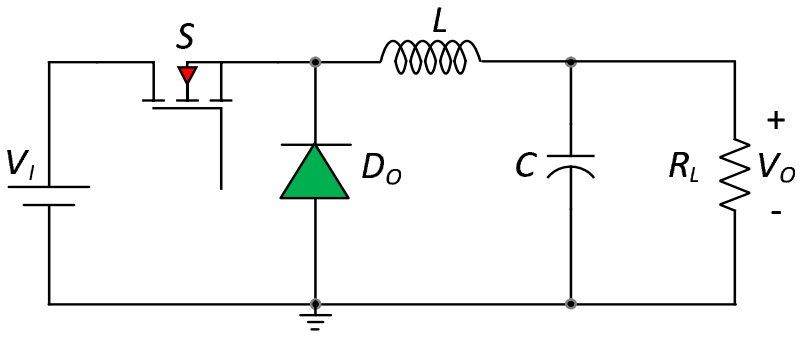

Figure 5.1: Circuit of the pulse-width modulated buck converter.

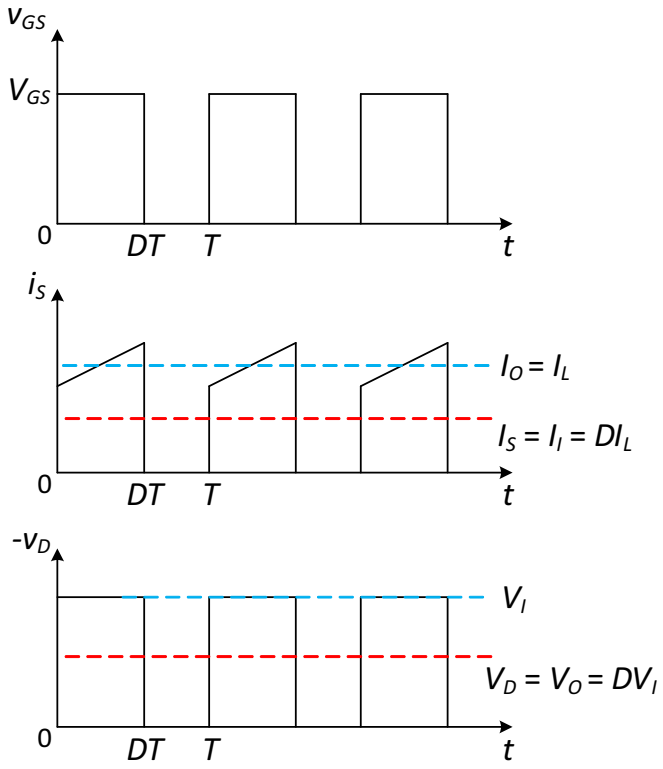

Figure 5.2: Waveforms of the ideal switching network. (a) gate-to-source voltage of switch (b) switch current, and (c) diode voltage.

and the dc current transfer function of the ideal converter is

$$M_{IDC} = \frac{I_O}{I_I} = \frac{1}{D}. \tag{5.6}$$

Fig. 5.3 shows the linearized dc and low frequency of buck dc-dc converter. Inductor is a short circuited and filter capacitor is open circuited in the dc model. This model describes the behavior of the converter at steady-state. The efficiency of the converter is

$$\begin{aligned}\eta &= \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = M_{IDC} M_{VDC} \\ &= \frac{1}{1 + \dfrac{Dr_{DS} + (1-D)R_F + r_L}{R_L} + \dfrac{(1-D)V_F}{V_O} + \dfrac{f_s C_o R_L}{M_{VDC}^2} + \dfrac{r_C R_L (1-D)^2}{12 f_s^2 L^2}}.\end{aligned} \tag{5.7}$$

where r_L, r_{DS}, V_F, R_F, r_C, C_o are the parasitic resistance of the inductor, ON-state resistance of the MOSFET, forward voltage of the diode, forward resistance of the

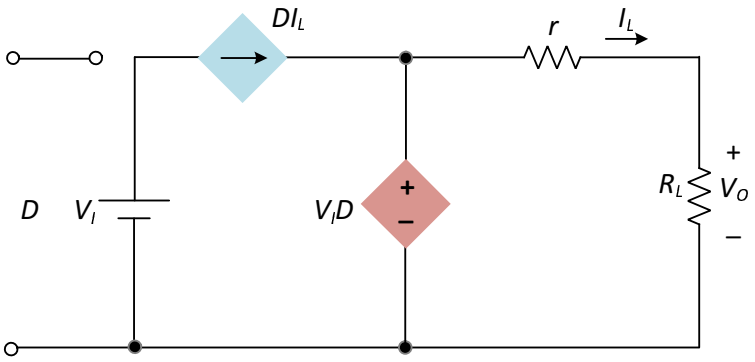

Figure 5.3: DC and low-frequency model of pulse-width-modulated buck dc-dc converter.

diode, equivalent series resistance of the filter capacitor, and output capacitance of the MOSFET, respectively.

5.2 Small-Signal Model of PWM Buck Converter in CCM

The averaged model is perturbed about the steady-state operating point resulting in large-signal nonlinear model. The large-signal quantities can be expressed as the sum of dc and ac components given by

$$i_S = I_S + i_s, \tag{5.8}$$

$$i_L = I_L + i_l, \tag{5.9}$$

$$v_D = V_D + v_d, \tag{5.10}$$

$$v_I = V_I + v_i, \tag{5.11}$$

$$v_O = V_O + v_o, \tag{5.12}$$

$$d_T = D + d, \tag{5.13}$$

where i_S, i_L, v_D, v_I, v_O, and d_T are the large-signal switch current, inductor current, diode voltage, input voltage, output voltage and duty cycle, respectively. The quantities i_s, i_l, v_d, v_i, v_o, and d are the small-signal switch current, inductor current, diode

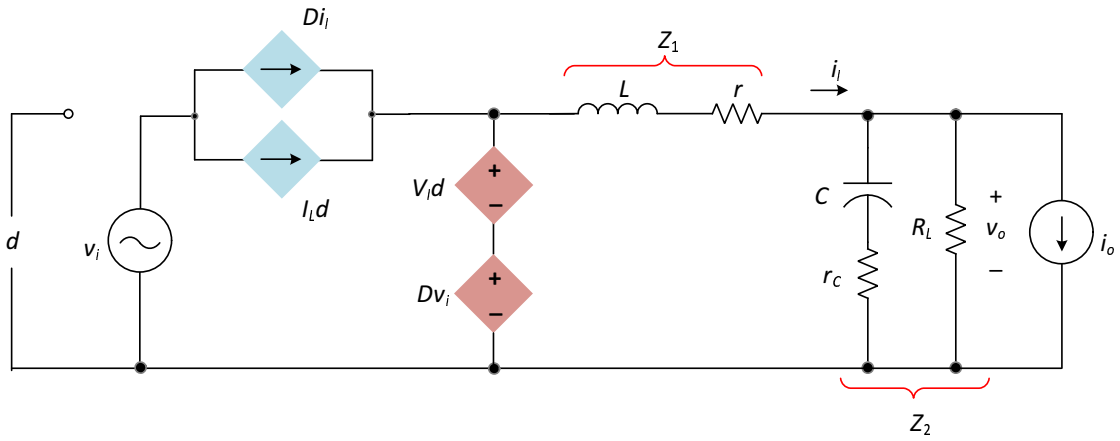

Figure 5.4: Small-signal model of the pulse-width-modulated buck dc-dc converter in continuous-conduction-mode (CCM).

voltage, input voltage, output voltage and duty cycle, respectively. Hence, from (5.1) and (5.2)

$$i_S = d_T i_L = (D + d)(I_L + i_l) \tag{5.14}$$

and

$$v_D = d_T v_I = (D + d)(V_I + v_i). \tag{5.15}$$

In (5.14) and (5.15), the high-order ac terms are eliminated by using the small signality conditions yielding a linearized large signal model. The dc and ac terms are separated to obtained dc averaged model as shown in Fig. 5.3 and the linear, averaged small-signal model as shown in Fig. 5.4. The equivalent averaged resistance r connected in series with the magnetizing inductance L is given as

$$r = r_{DS}D + (1 - D)R_F + r_L. \tag{5.16}$$

5.3 Design Example

The subsequent analysis is done on the buck converter designed for the following specifications.

1. Supply voltage $V_I = 28$ V.

2. Output voltage $V_O = 14$ V.

3. Output power $P_O = 20$ W.

4. Load resistance $R_L = 10\ \Omega$.

5. Switching frequency $f_s = 100$ kHz.

6. The inductance to ensure CCM operation is $L = 301\ \mu$H.

7. The capacitance to ensure CCM operation is $C = 68\ \mu$F.

The equivalent series resistances of the inductor is $r_L = 0.19\ \Omega$ and the capacitor is $r_C = 0.11\ \Omega$. The selected MOSFET was IRF540 by International Rectifiers and the selected diode was MBR10100 by Vishay Semiconductors. From their respective datasheets, the ON-state resistance of the MOSFET and the on-resistance of the diode were $r_{DS} = 0.11\ \Omega$, $R_F = 0.022\ \Omega$, and the output capacitance of the MOSFET is $C_o = 100\ p$F. Diode forward voltage is $V_F = 0.7$ V. The calculated value of converter efficiency is $\eta = 90\%$. The required duty cycle to achieve the rated output voltage

Table 5.1: Summary of calculated values for dc quantities

Variable	**Value**
I_I	0.78 A
I_O	1.4 A
M_{IDC}	1.8
M_{VDC}	0.5
D	0.5556
I_L	1.4 A
I_S	0.78 A
V_D	15.56 V

is $D = 0.5556$. The equivalent averaged resistance $r \approx 0.2998\ \Omega$. The open-loop dc quantities from 5.1 are given in Table 5.1.

5.4 Power Stage Transfer Functions

The following power stage transfer functions are discussed in the subsequent section.

1. Duty cycle-to-output voltage transfer function T_p.
2. Duty cycle-to-inductor current transfer function T_{pi}.
3. Input voltage-to-output voltage transfer function M_v.
4. Input voltage-to-inductor current transfer function M_{vi}.
5. Reverse current gain A_i.
6. Input impedance Z_i.
7. Output impedance Z_o.

The small-signal model of the PWM buck converter is shown in Fig. 5.4. The current through the parallel combination of the load resistance and the filter capacitor is

$$i_{Z2} = \frac{v_o}{Z_2}. \tag{5.17}$$

The current through the inductor is

$$i_l = \frac{Dv_i + V_I d}{Z_1 + Z_2}. \tag{5.18}$$

The input and the switch currents are

$$i_i = i_s = Di_l + I_L d. \tag{5.19}$$

Applying Kirchhoff's voltage law, the output voltage is

$$v_o = (Dv_i + V_I d)\frac{Z_2}{Z_1 + Z_2}. \tag{5.20}$$

The impedances Z_1 and Z_2 are

$$Z_1 = r + sL \tag{5.21}$$

and

$$Z_2 = R_L || \left(r_c + \frac{1}{sC} \right) = \frac{R_L \left(r_C + \frac{1}{sC} \right)}{R_L + r_C + \frac{1}{sC}}. \tag{5.22}$$

5.4.1 Duty Cycle-to-Output Voltage Transfer Function T_p

The duty cycle-to-output voltage transfer function is obtained by setting $v_i = 0$ and $i_o = 0$ in Fig. 5.4. Setting v_i in (5.20) and rearranging

$$v_o = V_I d \frac{Z_2}{Z_1 + Z_2}. \tag{5.23}$$

Hence, the control-to-output transfer function is

$$\begin{aligned} T_p(s) = \left. \frac{v_o(s)}{d(s)} \right|_{v_i = i_o = 0} \\ = V_I \frac{Z_2}{Z_1 + Z_2}. \end{aligned} \tag{5.24}$$

Substituting (5.21) and (5.22) in (5.24) gives the control-to-output transfer function in s-domain as

$$T_p(s) = \left. \frac{v_o(s)}{d(s)} \right|_{v_i = i_o = 0} = T_{px} \frac{(s + \omega_{zn})}{s^2 + 2\xi\omega_o s + \omega_o^2} = T_{po} \frac{\left(1 + \frac{s}{\omega_{zn}} \right)}{\left(\frac{s}{\omega_o} \right)^2 + \frac{2\xi s}{\omega_o} + 1}, \tag{5.25}$$

where the dc gain T_{po} is

$$T_{po} = \frac{V_I R_L}{R_L + r}, \tag{5.26}$$

the gain T_{px} is

$$T_{px} = \frac{V_I R_L r_C}{L(R_L + r_C)}, \tag{5.27}$$

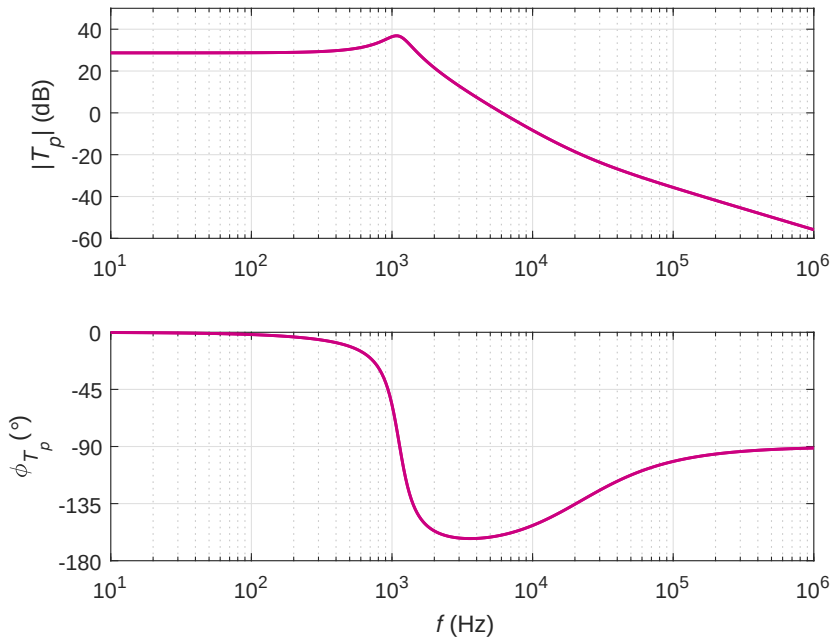

Figure 5.5: Theoretically obtained magnitude and phase plots of the duty cycle-to-output voltage transfer function T_p.

the angular corner frequency or the angular undamped natural frequency is

$$\omega_o = \sqrt{\frac{R_L + r}{LC(R_L + r_C)}}, \tag{5.28}$$

the damping ratio is

$$\xi = \frac{L + C[R_L(r_C + r) + r_C r]}{2\sqrt{LC(R_L + r_C)(R_L + r)}}, \tag{5.29}$$

and the angular frequency of the left-half plane zero is

$$\omega_{zn} = \frac{1}{r_C C}. \tag{5.30}$$

Fig. 5.5 shows the theoretically obtained magnitude and phase plots of duty-cycle-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 5.6 shows the magnitude and phase plots of duty-cycle-to-output voltage transfer function using SABER Simulator. The gain at dc and low-frequencies is nearly $T_{p0} = 30$ dB $= 31.2$ V/V. The natural corner frequency of the second-order low-pass filter formed by the inductor, capacitor, and load resistor is $f_o =$

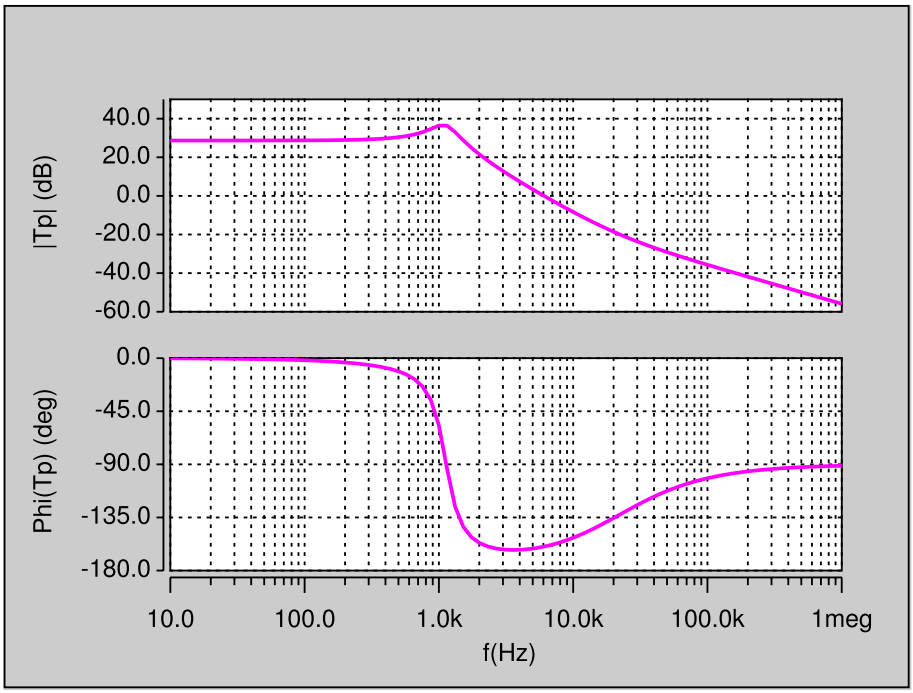

Figure 5.6: Magnitude and phase plots of the duty cycle-to-output voltage transfer function T_p obtained by circuit simulations.

1.1 kHz. The gain decreases by 40 dB/dec beyond f_o up to the zero frequency f_z. The zero frequency is caused by the series combination of the filter capacitance and the equivalent series resistance of the filter capacitance. The phase is 0° at dc and low frequencies indicating a zero phase inversion between the duty cycle and the output voltage, i.e., as duty cycle increases or decreases, the output voltage increases or decreases, respectively. At high frequencies, the phase flattens at −90° due to the zero frequency f_z. The phase dips towards −180° and achieves a minimum value of −150° at 3.2 kHz. The minimum phase depends largely on the load resistance R_L. Smaller is the load resistance, closer is the phase to −180°. At lower load resistance, the damping coefficient is small, the phase is nearly −180° and the buck converter producing ringing in the output voltage waveform of frequency f_o. Therefore, a buck converter in continuous-conduction mode must always have a minimum load in order to minimize ringing to about 2-3 oscillations and ensure satisfactory closed-loop

stability.

5.4.2 Duty Cycle-to-Inductor Current Transfer Function T_{pi}

The duty cycle-to-inductor current transfer function is obtained by setting $v_i = 0$ and $i_o = 0$ in Fig. 5.4. Setting $v_i = 0$ in (5.18) and rearranging

$$i_l = \frac{V_I d}{Z_1 + Z_2}. \tag{5.31}$$

Hence, the control-to-inductor current transfer function is

$$T_{pi}(s) = \left.\frac{i_l(s)}{d(s)}\right|_{v_i=i_o=0} = \frac{V_I}{Z_1 + Z_2}. \tag{5.32}$$

Substituting (5.21) and (5.22) in (5.32) gives the control-to-inductor current transfer function in s-domain as

$$T_{pi}(s) = \left.\frac{i_l(s)}{d(s)}\right|_{v_i=i_o=0} = T_{pix}\frac{(s+\omega_{zi})}{s^2 + 2\xi\omega_o s + \omega_o^2} = T_{pio}\frac{\left(1 + \dfrac{s}{\omega_{zi}}\right)}{\left(\dfrac{s}{\omega_o}\right)^2 + \dfrac{2\xi s}{\omega_o} + 1}, \tag{5.33}$$

where the dc gain T_{pio} is

$$T_{pio} = \frac{V_I}{R_L + r}, \tag{5.34}$$

the gain T_{pix} is

$$T_{pix} = \frac{V_I}{L}, \tag{5.35}$$

and the angular frequency of the left-half plane zero is

$$\omega_{zi} = \frac{1}{C(R_L + r_C)}. \tag{5.36}$$

Fig. 5.7 shows the theoretically obtained magnitude and phase plots of duty cycle-to-inductor current transfer function. The theoretical results were validated by simulation. Fig. 5.8 shows the magnitude and phase plots of duty cycle-to-inductor current transfer function using SABER Simulator. The gain at dc and low-frequencies

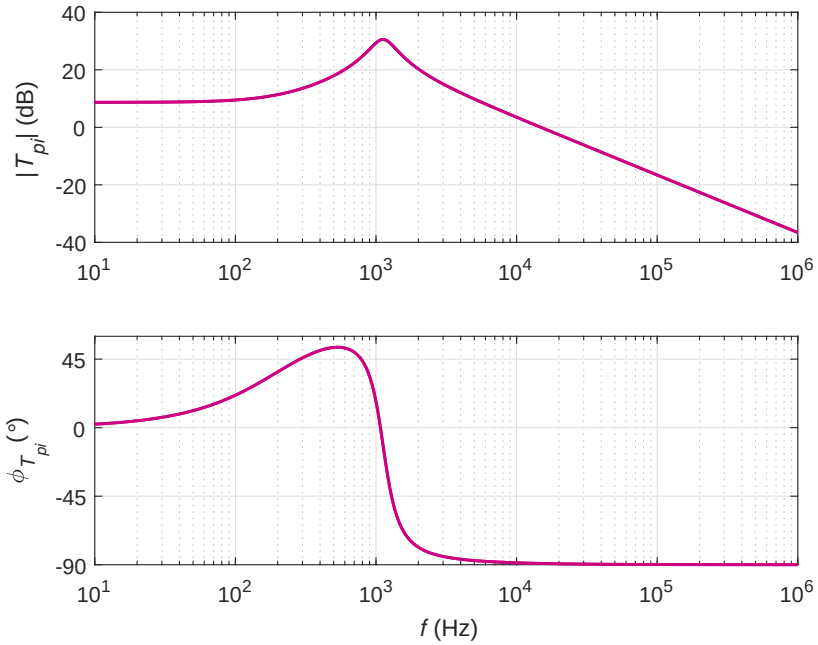

Figure 5.7: Theoretically obtained magnitude and phase plots of the duty cycle-to-inductor current transfer function T_{pi}.

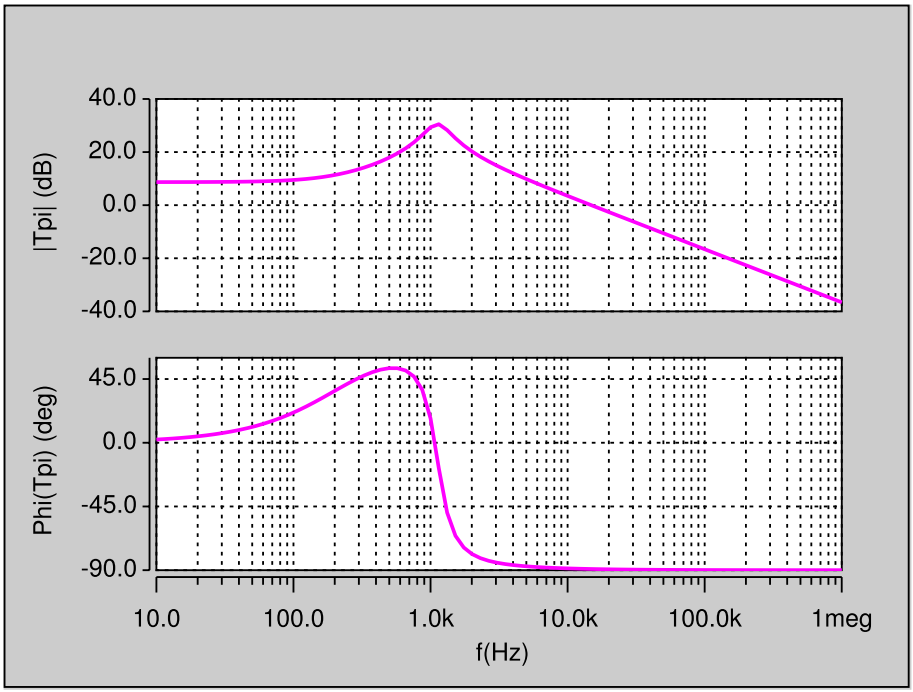

Figure 5.8: Magnitude and phase plots of the duty cycle-to-inductor current transfer function T_{pi} obtained by circuit simulation.

is nearly $T_{pi0} = 8.94$ dB $= 2.8$ A/V. The natural corner frequency of the second-order low-pass filter formed by the inductor, capacitor, and load resistor is $f_o = 1.1$ kHz. The frequency of the left-half plane zero is $f_{zi} =$. The gain decreases at the rate of 20 dB/dec beyond f_o. The duty cycle-to-inductor current transfer function for the buck converter exhibits a low-frequency zero f_{zi} and a complex conjugate pole-pair at f_o. The phase starts at zero and rises to 45° due to f_{zi}. This means that at low frequencies, the duty cycle signal leads the inductor current by a particular phase angle. The bandwidth of T_{pi} is larger than that of T_p. Therefore, the inner current loop presents a faster response in inductor current for change in duty cycle. The low-frequency zero f_{zi} depends on the load resistance R_L and the parameters of the filter capacitance, namely C and r_C. As the value of R_L is decreased at a fixed C, f_{zi} moves towards f_o. The nature of the roots of the characteristic equation (denominator of T_{pi}) or the poles of T_{pi} converts from complex conjugate to real. At a specific minimum load resistance, $f_{zi} \approx f_o$, i.e., f_{zi} cancels the effect of one of the complex conjugate poles at f_o producing a first-order dominant pole system. The dominant pole is therefore caused by the inductor and load resistance.

5.4.3 Input Voltage-to-Output Voltage Transfer Function M_v

The input voltage-to-output voltage transfer function is obtained by setting $d = 0$ and $i_o = 0$ in Fig. 5.4. Setting $d = 0$ in (5.20) and rearranging

$$v_o = D v_i \frac{Z_2}{Z_1 + Z_2}. \tag{5.37}$$

Hence, the input voltage-to-output voltage transfer function M_v

$$M_v(s) = \left.\frac{v_o(s)}{v_i(s)}\right|_{d=i_o=0} = D\frac{Z_2}{Z_1 + Z_2}. \tag{5.38}$$

Substituting (5.21) and (5.22) in (5.32) gives the input voltage-to-output voltage transfer function in s-domain as

$$M_v(s) = \frac{v_o(s)}{v_i(s)}\bigg|_{d=i_o=0} = M_{vx}\frac{(s+\omega_{zn})}{s^2+2\xi\omega_o s+\omega_o^2} = M_{vo}\frac{\left(1+\dfrac{s}{\omega_{zn}}\right)}{\left(\dfrac{s}{\omega_o}\right)^2+\dfrac{2\xi s}{\omega_o}+1}, \tag{5.39}$$

where the dc gain M_{vo} is

$$M_{vo} = \frac{DR_L}{R_L+r} \tag{5.40}$$

and the gain M_{vx} is

$$M_{vx} = \frac{DR_L r_C}{L(R_L+r_C)}. \tag{5.41}$$

The angular frequency of the left-half plane zero is given in (5.30).

Fig. 5.9 shows the theoretically obtained magnitude and phase plots of input voltage-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 5.10 shows the magnitude and phase plots of input voltage-to-output

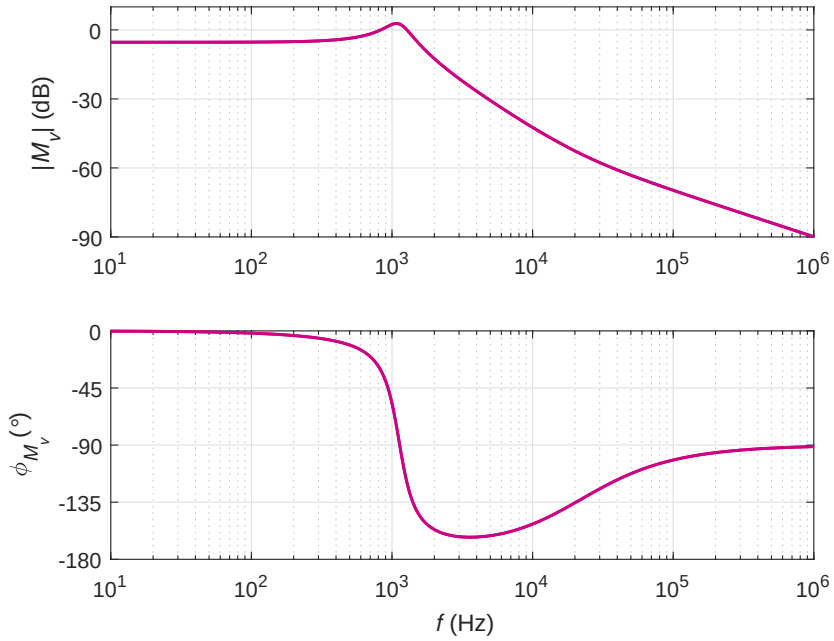

Figure 5.9: Theoretically obtained magnitude and phase plots of the input voltage-to-output voltage transfer function M_v.

voltage transfer function using SABER Simulator. The gain at dc is nearly equal to the duty cycle D. The open-loop buck converter inherently offers sufficient supply voltage rejection especially at low duty ratios. This is because, at low duty cycle the power supply is connected to the load only for a portion of the switching period, unlike in other dc-dc converter counterparts such as boost or buck-boost converters. The phase starts at zero and decreases towards $-180°$. However, the high-frequency LHP zero at ω_{zn} increases the phase to 90°.

5.4.4 Input Voltage-to-Inductor Current Transfer Function M_{vi}

The input voltage-to-inductor current transfer function is obtained by setting $d = 0$ and $i_o = 0$ in Fig. 5.4. Setting $d = 0$ in (5.18) and rearranging

$$i_l = \frac{Dv_i}{Z_1 + Z_2}. \tag{5.42}$$

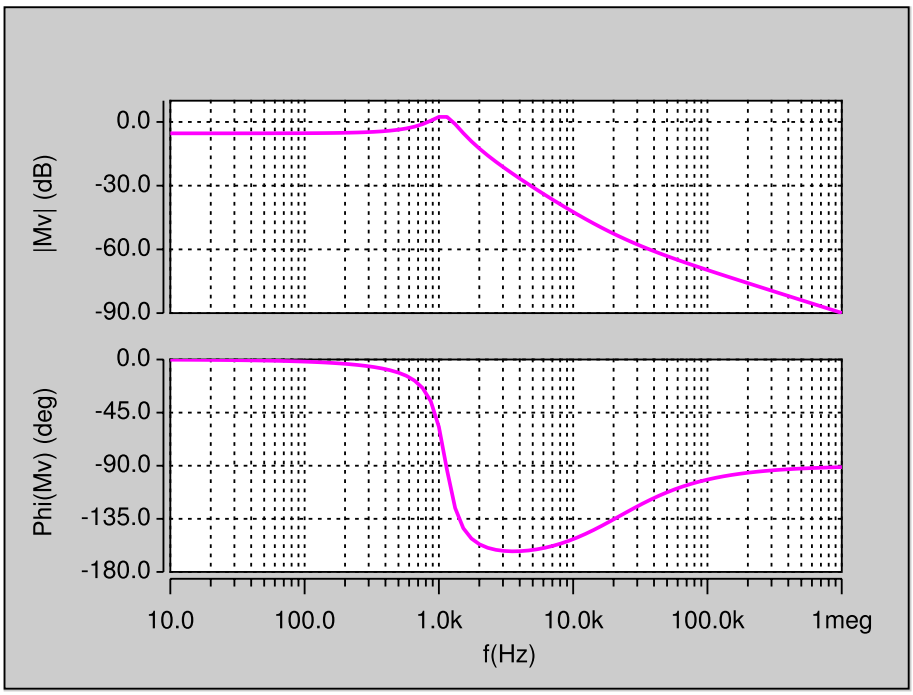

Figure 5.10: Magnitude and phase plots of the input voltage-to-output voltage transfer function M_v obtained by circuit simulation.

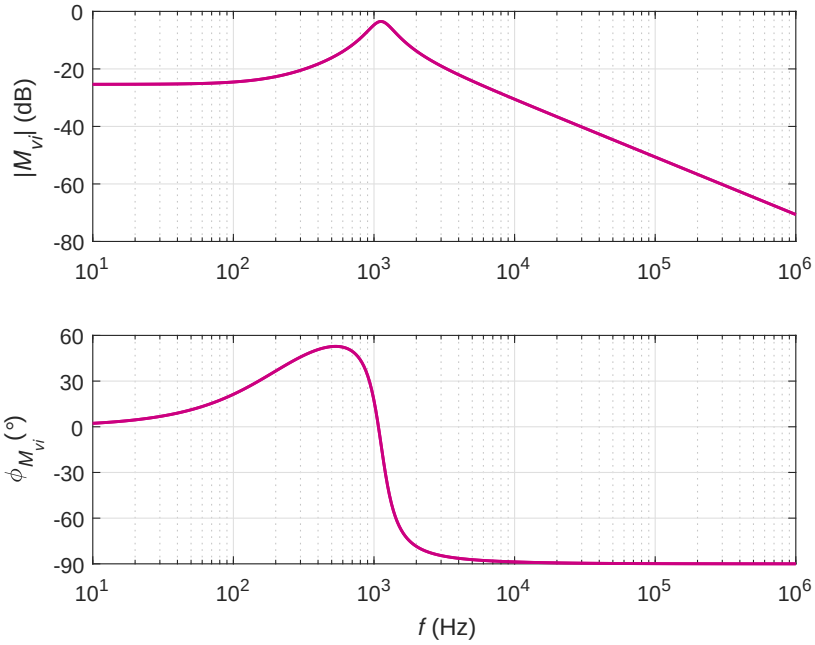

Figure 5.11: Theoretically obtained magnitude and phase plots of input voltage-to-inductor current transfer function M_{vi}.

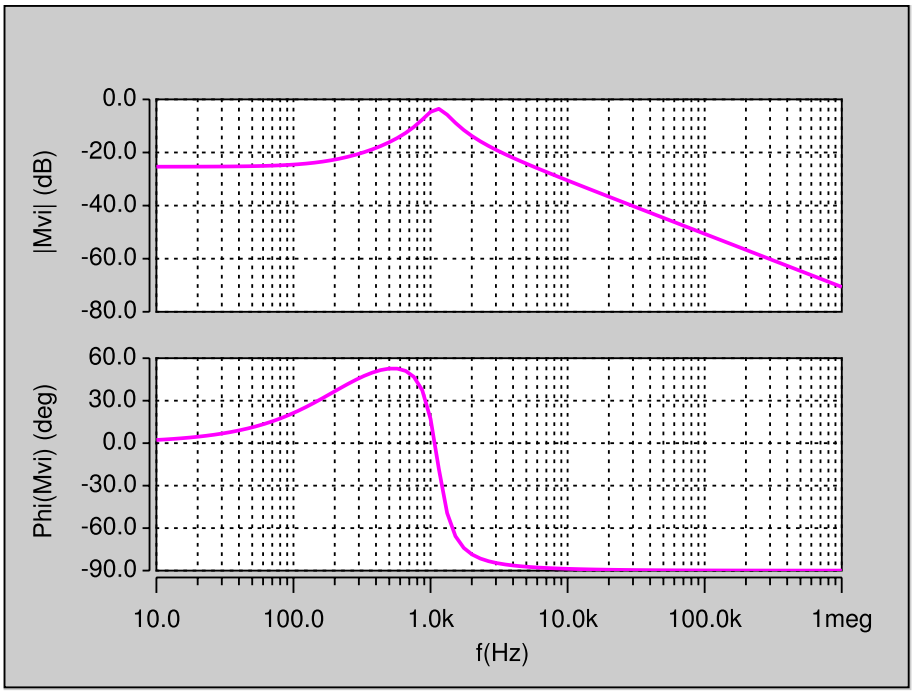

Figure 5.12: Magnitude and phase plots of input voltage-to-inductor current transfer function M_{vi} obtained by circuit simulation.

Hence, the input voltage-to-inductor current transfer function M_{vi} is

$$M_{vi}(s) = \left.\frac{i_l(s)}{v_i(s)}\right|_{d=i_o=0} = \frac{D}{Z_1 + Z_2}. \tag{5.43}$$

Substituting (5.21) and (5.22) in (5.43) gives the input voltage-to-inductor current transfer function in s-domain as

$$M_{vi}(s) = \left.\frac{i_l(s)}{v_i(s)}\right|_{d=i_o=0} = M_{vix}\frac{(s+\omega_{zi})}{s^2 + 2\xi\omega_o s + \omega_o^2} = M_{vio}\frac{\left(1 + \dfrac{s}{\omega_{zi}}\right)}{\left(\dfrac{s}{\omega_o}\right)^2 + \dfrac{2\xi s}{\omega_o} + 1}, \tag{5.44}$$

where the dc gain M_{vio} is

$$M_{vio} = \frac{D}{R_L + r}, \tag{5.45}$$

the gain M_{vix} is

$$M_{vix} = \frac{D}{L}, \tag{5.46}$$

and the angular frequency of the left-half plane zero is

$$\omega_{zi} = \frac{1}{C(R_L + r_C)}. \tag{5.47}$$

Fig. 5.11 shows the theoretically obtained magnitude and phase plots of input voltage-to-inductor current transfer function. The theoretical results were validated by simulation. Fig. 5.12 shows the magnitude and phase plots of input voltage-to-inductor current transfer function using SABER Simulator. The gain at dc is $M_{vi0} =$ dB $=$ V/V. Through the M_{vi} current-loop relevant transfer function, one can observe that the current loop offers a low audio susceptibility at dc than that provided by the voltage-loop transfer function M_v. All the other frequency-domain properties remain identical to T_{pi}

5.4.5 Reverse Current Gain A_i

The small-signal model to derive output-to-inductor current transfer function is shown in Fig. 5.13. This model is obtain by setting $v_i = 0$ and $d = 0$. An independent voltage source v_t is applied at the output, which forces a current i_t. Applying Kirchhoff's

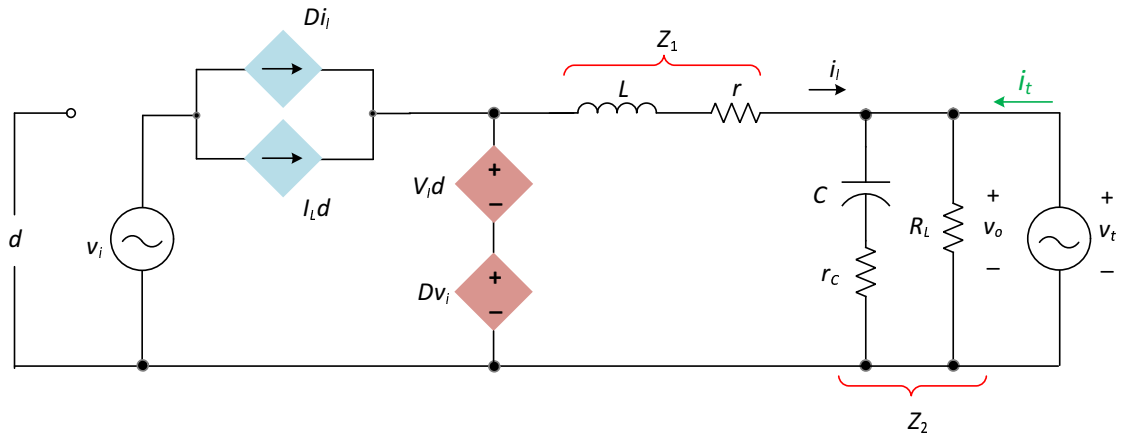

Figure 5.13: Small-signal model of the pulse-width modulated buck dc-dc converter in CCM to derive output current-to-inductor current transfer function A_i.

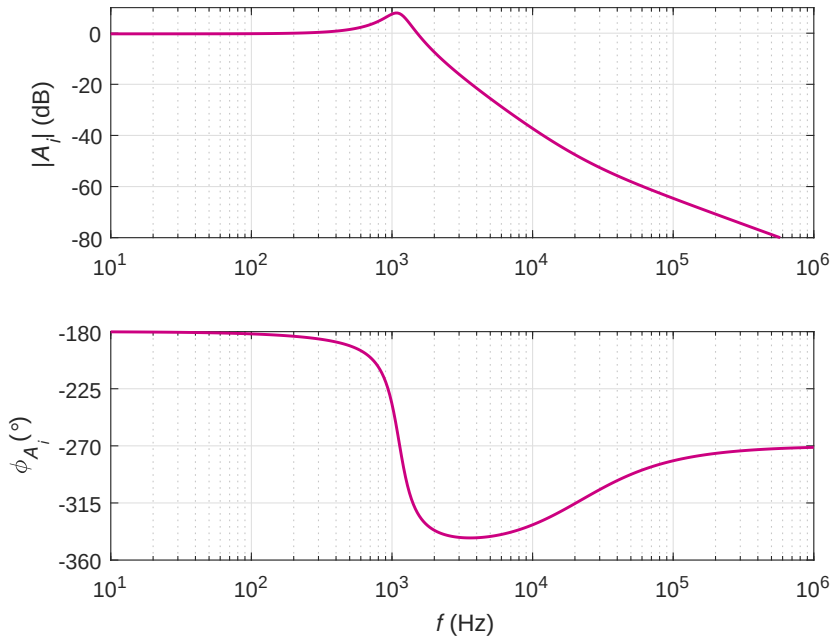

Figure 5.14: Theoretically obtained magnitude and phase plots of the output current-to-inductor current transfer function A_i.

voltage law,

$$v_o = -v_t = -i_l Z_1 \tag{5.48}$$

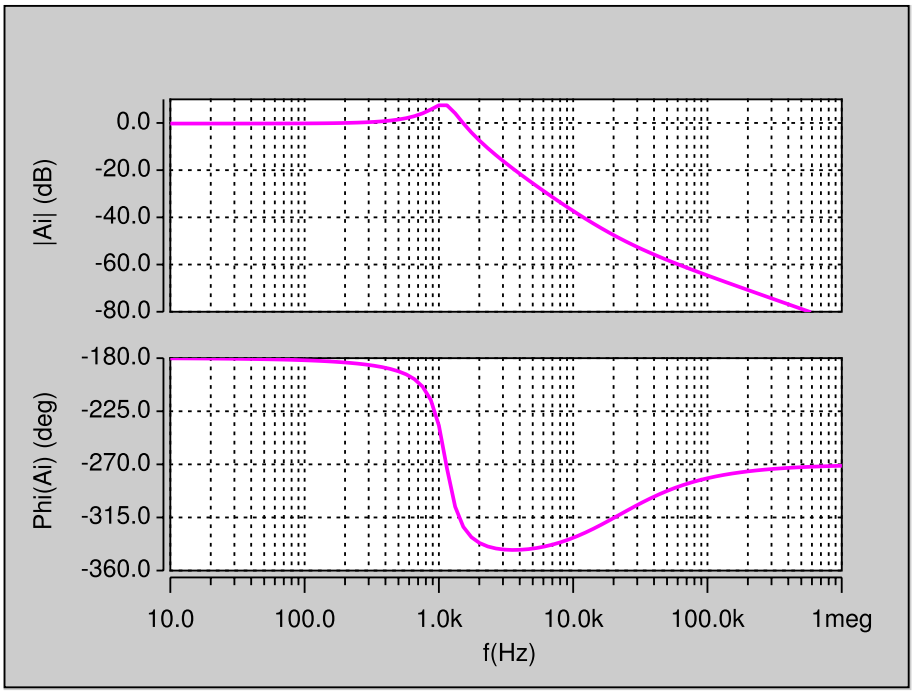

Figure 5.15: Magnitude and phase plots of the output current-to-inductor current transfer function A_i obtained by circuit simulation.

and

$$\begin{aligned} i_l &= i_o + \frac{v_o}{Z_2} = i_o + \frac{-i_l Z_1}{Z_2} \\ i_o &= i_l(1 + \frac{Z_1}{Z_2}) = i_l \frac{Z_1 + Z_2}{Z_2}. \end{aligned} \tag{5.49}$$

The current i_t is

$$i_t = -i_o = -i_l \frac{Z_1 + Z_2}{Z_2}. \tag{5.50}$$

Hence, the output current-to-inductor current transfer function or reverse current transfer function A_i is

$$A_i(s) = \left.\frac{i_l(s)}{i_o(s)}\right|_{d=v_i=0} = \frac{Z_2}{Z_1 + Z_2}. \tag{5.51}$$

Substituting (5.21) and (5.22) in (5.51) gives the output current-to-inductor current transfer function in s-domain as

$$A_i(s) = \left.\frac{i_l(s)}{i_o(s)}\right|_{d=v_i=0} = A_{ix} \frac{(s + \omega_{zn})}{s^2 + 2\xi\omega_o s + \omega_o^2} = A_{io} \frac{\left(1 + \dfrac{s}{\omega_{zn}}\right)}{\left(\dfrac{s}{\omega_o}\right)^2 + \dfrac{2\xi s}{\omega_o} + 1}, \tag{5.52}$$

where the dc gain A_{io} is

$$A_{io} = \frac{R_L}{R_L + r}, \tag{5.53}$$

the gain A_{ix} is

$$A_{ix} = \frac{R_L r_C}{L(R_L + r_C)}, \tag{5.54}$$

and the angular frequency of the left-half plane zero ω_{zn} is given in (5.30).

Fig. 5.14 shows the theoretically obtained magnitude and phase plots of output-to-inductor current transfer function. The theoretical results were validated by simulation. Fig. 5.15 shows the magnitude and phase plots of output-to-inductor current transfer function using SABER Simulator. The gain at dc is $A_{i0} = 0$ dB $= 1$ A/A, i.e., the reverse current gain is unity at dc and low-frequencies up to nearly f_o. Beyond f_o the impedance offered by the capacitor branch is lower than the inductor and the small-signal output current begins to flow into the capacitor. Therefore, the gain reduces by -40 dB per decade.

5.4.6 Open-Loop Input Impedance Z_i

The open-loop input impedance is obtained by setting $d = 0$ and $i_o = 0$ in (5.19) and (5.20) and rearranging as

$$i_i = D i_l \tag{5.55}$$

and

$$i_l = \frac{D v_i}{Z_1 + Z_2}, \tag{5.56}$$

yielding

$$i_i = D \frac{D v_i}{Z_1 + Z_2}. \tag{5.57}$$

Hence, the open-loop input impedance is

$$Z_i(s) = \left. \frac{v_i(s)}{i_i(s)} \right|_{d=i_o=0} = \frac{Z_1 + Z_2}{D^2}. \tag{5.58}$$

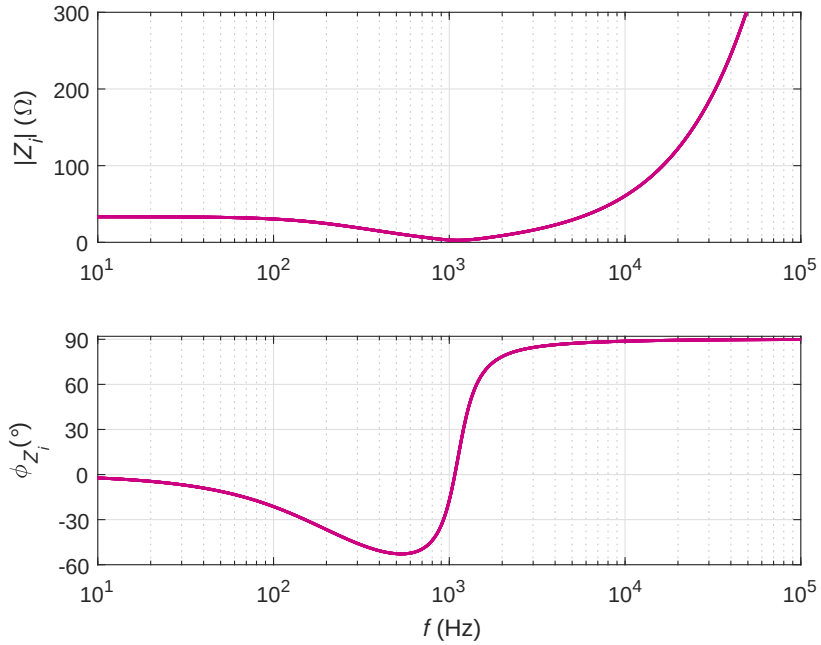

Figure 5.16: Theoretically obtained magnitude and phase plots of the input impedance Z_i.

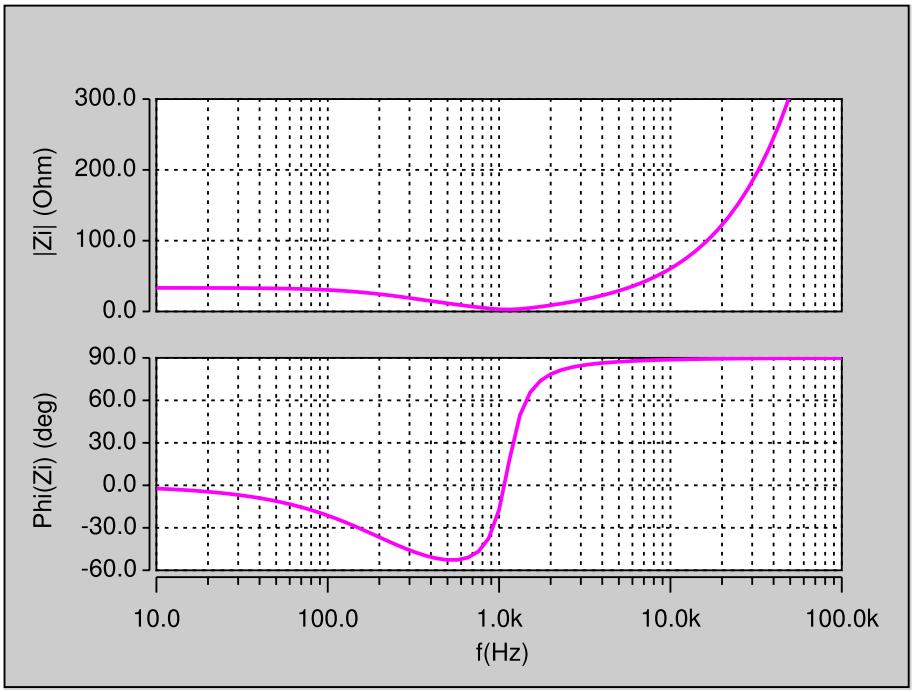

Figure 5.17: Magnitude and phase plots of the input impedance Z_i obtained by circuit simulation.

Substituting (5.21) and (5.22) in (5.58) gives the output current-to-inductor current transfer function in s-domain as

$$Z_i(s) = \left.\frac{v_i(s)}{i_i(s)}\right|_{d=i_o=0} = Z_{ix}\frac{s^2 + 2\xi\omega_o s + \omega_o^2}{(s+\omega_{zi})} = Z_{io}\frac{\left(\frac{s}{\omega_o}\right)^2 + \frac{2\xi s}{\omega_o} + 1}{\left(1 + \frac{s}{\omega_{zi}}\right)}, \tag{5.59}$$

where the dc gain Z_{io} is

$$Z_{io} = \frac{R_L + r}{D^2}, \tag{5.60}$$

the gain Z_{ix} is

$$Z_{ix} = \frac{L}{D^2}. \tag{5.61}$$

and the angular frequency of the left-half plane zero ω_{zi} is given in (5.47).

Fig. 5.16 shows the theoretically obtained magnitude and phase plots of input impedance. The theoretical results were validated by simulation. Fig. 5.17 shows the magnitude and phase plots of input impedance using SABER Simulator.

5.4.7 Open-Loop Output Impedance Z_o

The small-signal model to derive output impedance is shown in Fig. 5.13. This model is obtain by setting $v_i = 0$ and $d = 0$. The open-loop output impedance is

$$Z_o(s) = \left.\frac{v_o(s)}{i_t(s)}\right|_{d=i_o=0} = Z_1||Z_2. \tag{5.62}$$

Substituting (5.21) and (5.22) in (5.62) gives the open-loop output impedance in s-domain as

$$Z_o(s) = \left.\frac{v_o(s)}{i_o(s)}\right|_{d=i_o=0} = Z_{ox}\frac{(s+\omega_{zn})(s+\omega_{rl})}{s^2 + 2\xi\omega_o s + \omega_o^2} = Z_{o0}\frac{\left(1 + \frac{s}{\omega_{zn}}\right)\left(1 + \frac{s}{\omega_{rl}}\right)}{\left(\frac{s}{\omega_o}\right)^2 + \frac{2\xi s}{\omega_o} + 1}, \tag{5.63}$$

where the dc gain Z_{o0} is

$$Z_{o0} = \frac{rR_L}{r + R_L}, \tag{5.64}$$

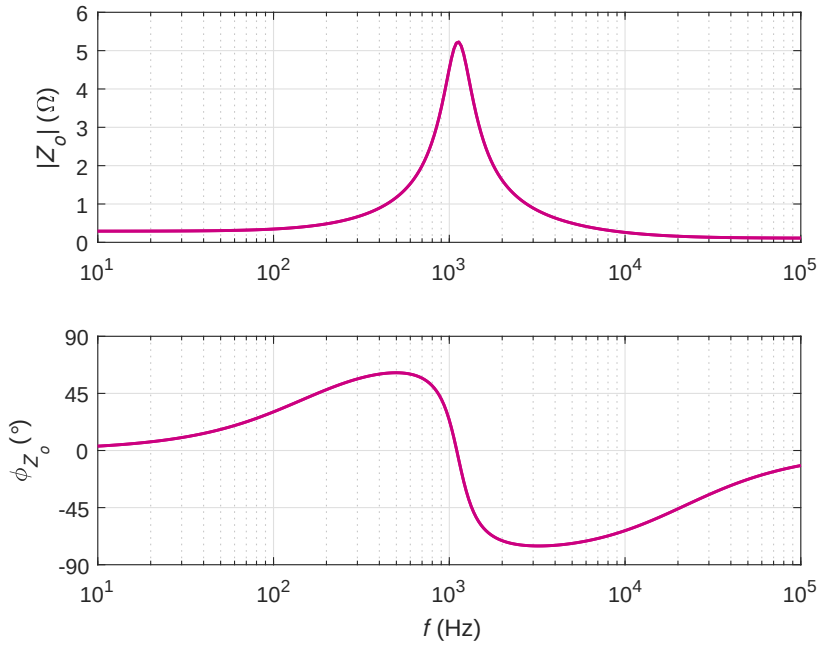

Figure 5.18: Theoretically obtained magnitude and phase plots of the output impedance Z_o.

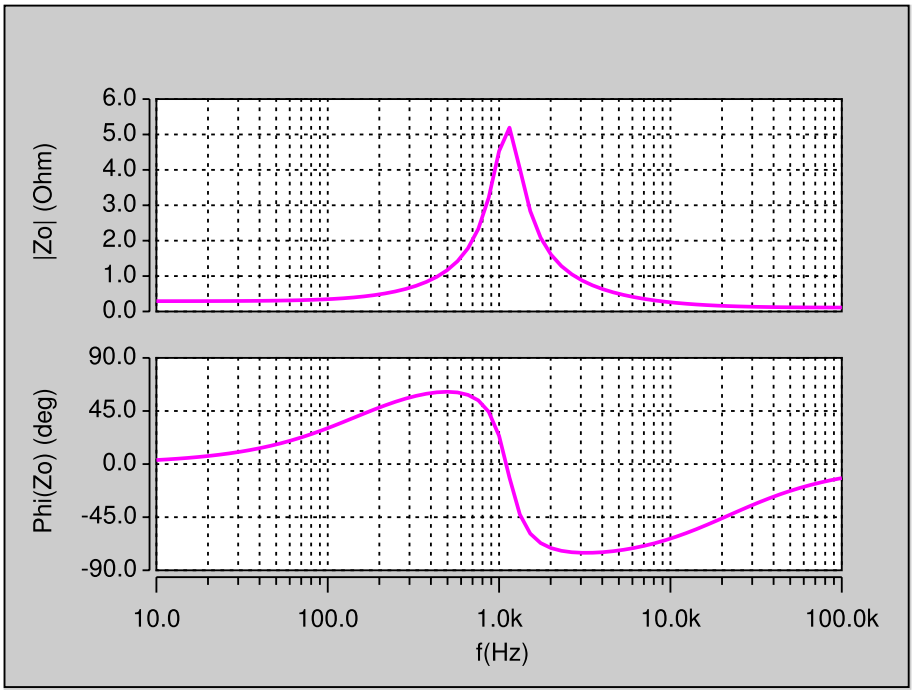

Figure 5.19: Magnitude and phase plots of the output impedance Z_o obtained by circuit simulation.

Table 5.2: Summary of calculated values for open-loop transfer functions

Variable	**Value**
$\|T_{po}\|$	$27.19 = 28.69$ dB
$\|T_{pio}\|$	$2.72 = 24.32$ dB
$\|M_{vo}\|$	$0.539 = -5.37$ dB
$\|M_{vio}\|$	$0.054 = -25.35$ dB
$\|Z_{io}\|$	$33.37 = -30.467$ dB
$\|Z_{oo}\|$	$0.2911 = -10.72$ dB
ω_o	7.05 krad/s
f_o	1.123 kHz
ξ	0.199
ω_{zi}	1.454 krad/s
f_{zi}	231.5 kHz
ω_{zn}	133.7 krad/s
f_z	21.28 kHz
ω_{rl}	995.93 krad/s
f_{rl}	158.5 kHz

the gain Z_{ox} is

$$Z_{ox} = \frac{R_L r_C}{R_L + r_C}, \tag{5.65}$$

and the angular frequency of the left-half plane zero ω_{rl} is

$$\omega_{rl} = \frac{r}{L}. \tag{5.66}$$

The angular frequency of the left-half plane zero ω_{zn} is given in (5.30).

Fig. 5.18 shows the theoretically obtained magnitude and phase plots of output impedance. The theoretical results were validated by simulation. Fig. 5.19 shows the magnitude and phase plots of output impedance using SABER Simulator.

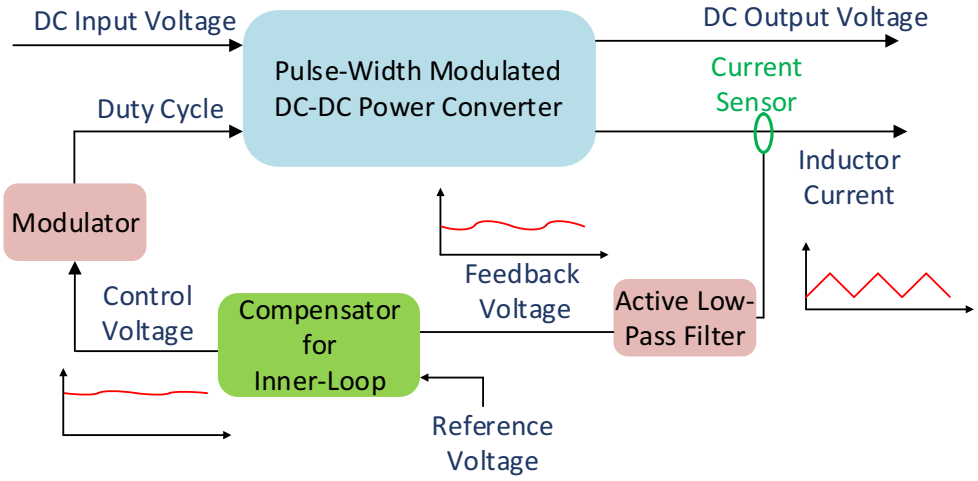

Figure 5.20: Architecture of the inner-current loop with filter.

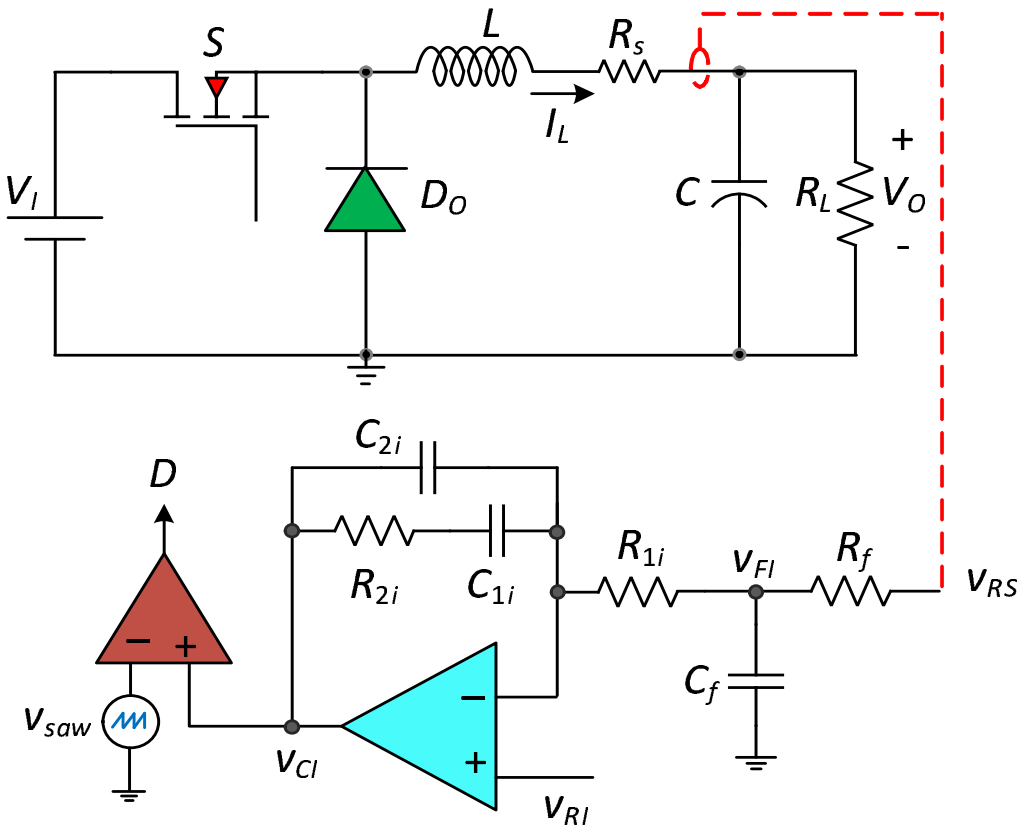

Figure 5.21: Circuit of buck dc-dc converter with inner-current loop.

5.5 Inner-Current Loop

5.5.1 Transfer Function of Filter and Non-Inverting Amplifier T_f

The low-pass filter stage is composed of a resistor R_f and a capacitor C_f, placed in series with the non-inverting amplifier. The non-inverting amplifier is composed of two resistors R_{af1} and R_{af}. The transfer function of two stages is

$$\begin{aligned} T_f(s) = \frac{v_{fi}(s)}{v_{rs}(s)} = \frac{Z_{Cf}}{Z_{Cf} + R_f} = \frac{\frac{1}{sC_f}}{\frac{1}{sC_f} + R_f} = \frac{1}{1 + sR_fC_f} \\ = \frac{1}{R_fC_f} \frac{1}{s + \frac{1}{R_fC_f}} = \frac{\omega_{pf}}{s + \omega_{pf}} = \frac{1}{\frac{s}{\omega_{pf}} + 1}. \end{aligned} \tag{5.67}$$

$$T_f(s) = \frac{1}{\frac{j\omega}{\omega_{pf}} + 1}, \tag{5.68}$$

Rearranging

$$T_f\left(\frac{j\omega + \omega_{pf}}{\omega_{pf}}\right) = 1, \tag{5.69}$$

$$T_f(j\omega + \omega_{pf}) = \omega_{pf}, \tag{5.70}$$

Further modifications results in

$$\omega_{pf} = \frac{jT_f\omega}{1 - T_f} \tag{5.71}$$

and hence,

$$f_{pf} = \frac{jT_f f}{1 - T_f}. \tag{5.72}$$

Therefore, the filter upper cutoff frequency can be obtained as

$$f_{pf} = \frac{T_f f}{1 - T_f}. \tag{5.73}$$

The filter frequency can be set by the amount of attenuation desired. For an example, to achieve an attenuation of 33% in the filter output voltage at the switching frequency, i.e., $|T_f|(f_s) = 0.33$, the filter upper cutoff frequency using (5.73) must be $f_{pf} = 0.5f_s = 50$ kHz.

5.5.2 Transfer Function of Pulse-Width Modulator T_m

The control voltage-to-duty cycle transfer function of the pulse-width modulator is

$$T_m = \frac{D}{V_C} = \frac{d}{v_c} = \frac{1}{V_{Tm}}, \tag{5.74}$$

where V_{Tm} is the amplitude of the sawtooth waveform.

5.5.3 Uncompensated Loop Gain T_{ki}

The natural behavior of the inner current loop can be determined using the uncompensated loop gain as

$$T_{ki} = \frac{v_{fi}}{v_{ei}} = T_m T_{pi} R_s T_f = T_{ki0} \frac{\left(1 + \frac{s}{\omega_{zi}}\right)}{\left(1 + \frac{s}{\omega_{pf}}\right)\left(1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}\right)}, \tag{5.75}$$

where T_m, T_{pi} and T_f are given in (5.74), (5.33), and (5.67), respectively. The dc gain T_{ki0} is given by

$$T_{ki0} = \frac{R_s}{V_{Tm}} \frac{V_I}{R_L + r}. \tag{5.76}$$

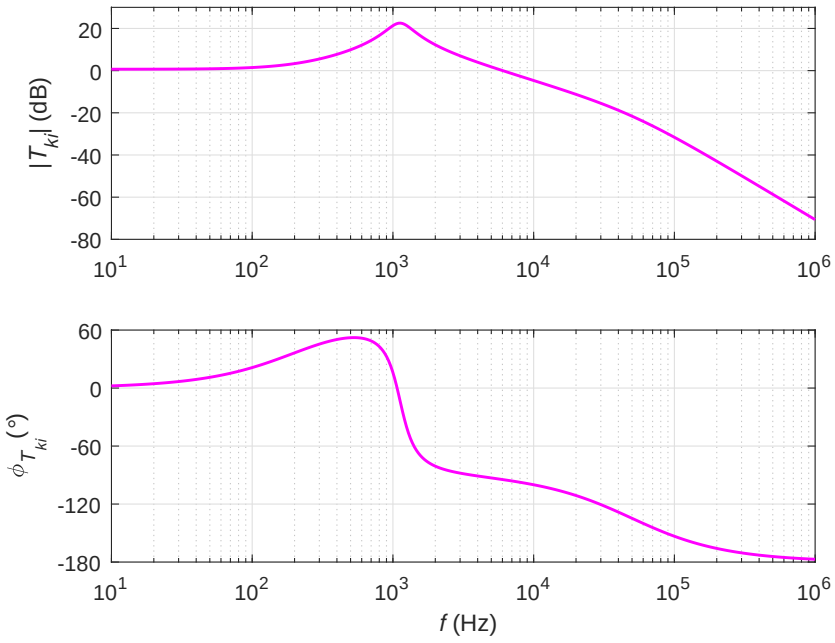

Figure 5.22: Theoretically obtained magnitude and phase plots of the uncompensated loop gain T_{ki} of inner-current loop.

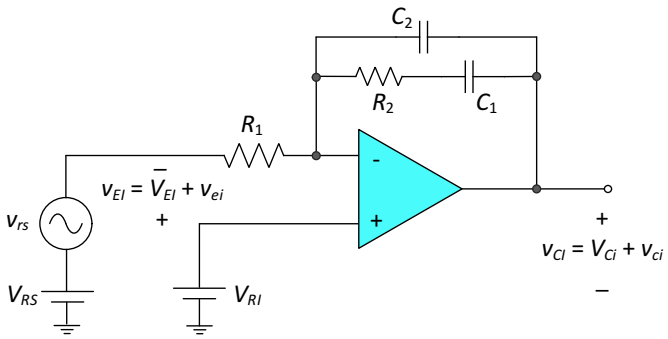

Figure 5.23: Circuit of type-II compensator.

Fig. 5.22 shows the theoretically obtained magnitude and phase plots of the uncompensated loop gain of the inner-current loop.

5.5.4 Transfer Function of Control Circuit T_{ci}

An integral-single-lead control circuit introduces a pole at the origin required to boost the dc gain and a pole-zero pair to adjust crossover frequency f_c to maintain required

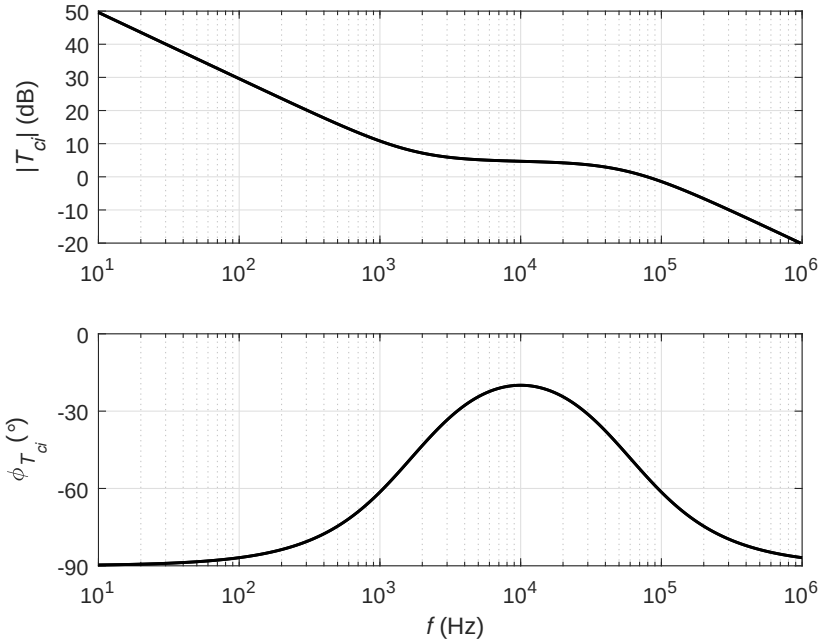

Figure 5.24: Theoretically obtained magnitude and phase plots of controller transfer function T_{ci} for the inner-current loop.

PM. A detailed procedure to determine the transfer function of the controller to improve the dc gain ($>$ 50 dB) and achieve an inner current loop phase margin $PM = 60°$ is explained in [34] and only the relevant expressions are presented here. The transfer function T_{ci} of the current loop control circuit is

$$T_{ci} = \frac{v_{ci}(s)}{v_{ei}(s)} = T_{cio} \frac{1 + \dfrac{s}{\omega_{zci}}}{s\left(1 + \dfrac{s}{\omega_{pci}}\right)}, \tag{5.77}$$

where

$$T_{cio} = \frac{1}{R_1(C_1 + C_2)}, \tag{5.78}$$

$$\omega_{zci} = \frac{1}{R_2 C_1}, \tag{5.79}$$

and

$$\omega_{zci} = \frac{(C_1 + C_2)}{R_2 C_1 C_2}. \tag{5.80}$$

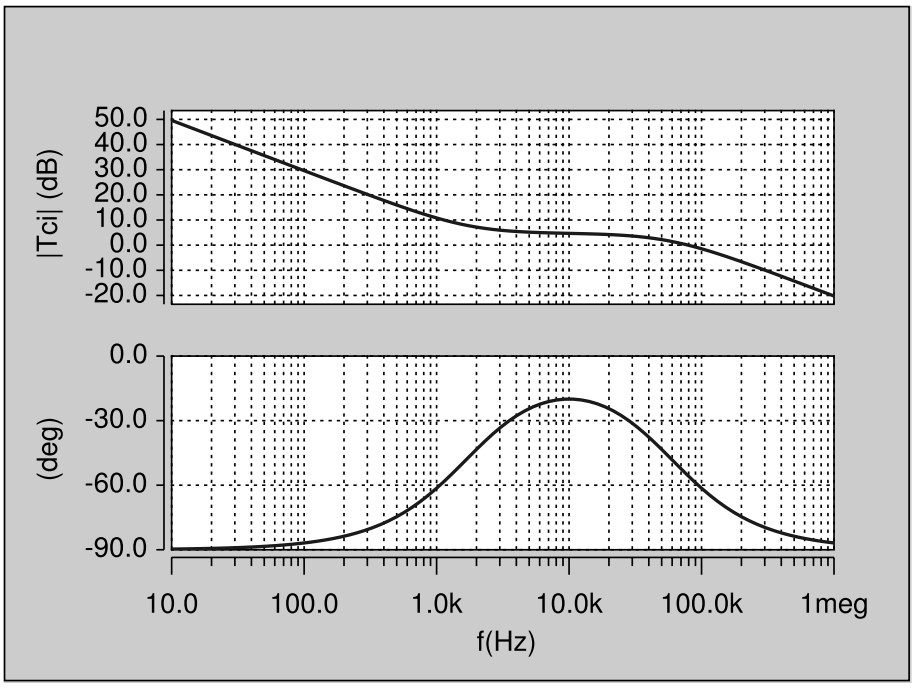

Figure 5.25: Magnitude and phase plots of output impedance obtained by circuit simulation of controller transfer function T_{ci} for the inner-current loop.

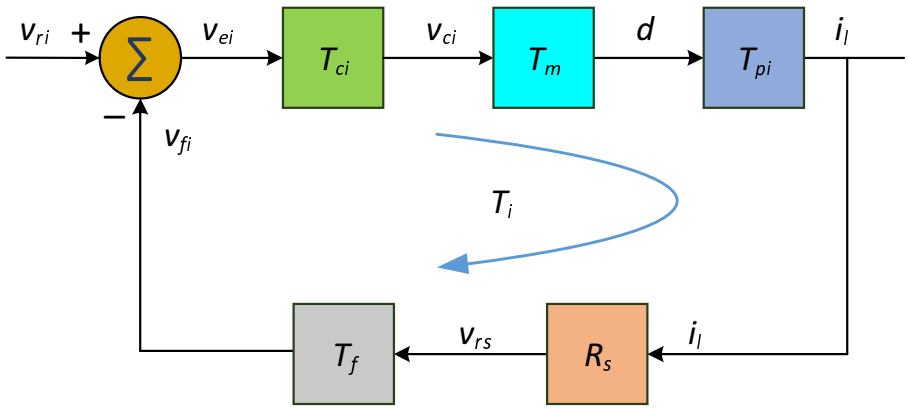

Figure 5.26: Block diagram of inner-current loop.

Fig. 5.24 shows the theoretically obtained magnitude and phase plots of the compensator transfer function used in the inner-current loop. The theoretical results were validated by simulation. Fig. 5.25 shows the magnitude and phase plots of the compensator transfer function used in the inner-current loop using SABER Simulator.

5.5.5 Compensated Loop Gain of Inner-Current Loop T_i

The loop gain of the compensated inner-current loop is

$$T_i = \frac{v_{ei}}{v_{fi}} = T_{ki}T_{ci} = T_m T_{pi} R_s T_f T_{ci}, \tag{5.81}$$

to yield

$$T_i = T_{i0}\frac{(1+\frac{s}{\omega_{zi}})(1+\frac{s}{\omega_{zci}})}{s(1+\frac{s}{\omega_{pf}})(1+\frac{s}{\omega_{pci}})(1+\frac{2\xi s}{\omega_o}+\frac{s^2}{\omega_o^2})}, \tag{5.82}$$

where T_{i0} is the gain at $s = 0$ given as

$$T_{i0} = T_{ki0}T_{ci0} = \frac{V_I R_s}{V_{Tm}(R_L + r)}\frac{1}{R_1(C_1 + C_2)}. \tag{5.83}$$

Fig. 5.27 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop. The theoretical results were validated by simulation. Fig. 5.28 shows the magnitude and phase plots of compensated loop gain of the inner-current loop using SABER Simulator.

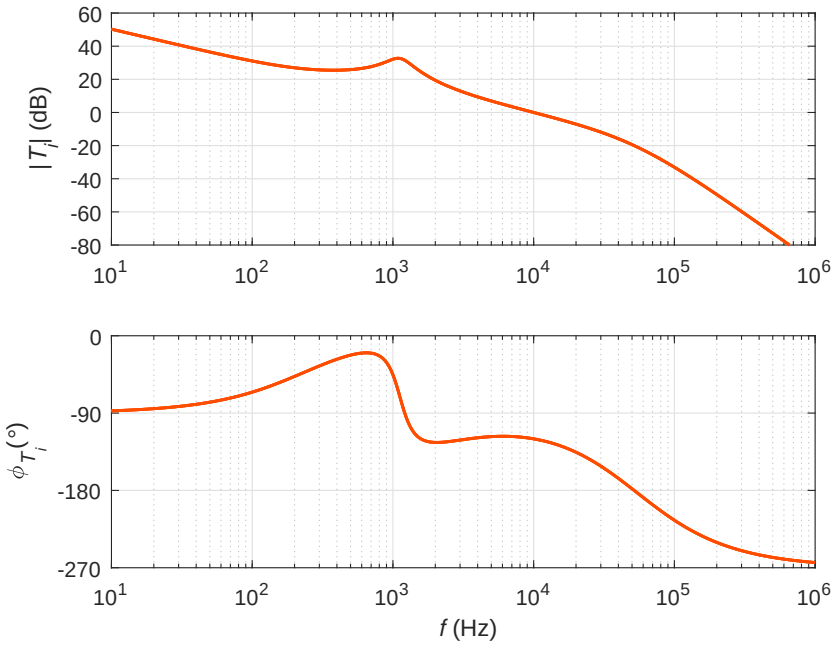

Figure 5.27: Theoretically obtained magnitude and phase plots of compensated loop gain T_i of the inner-current loop.

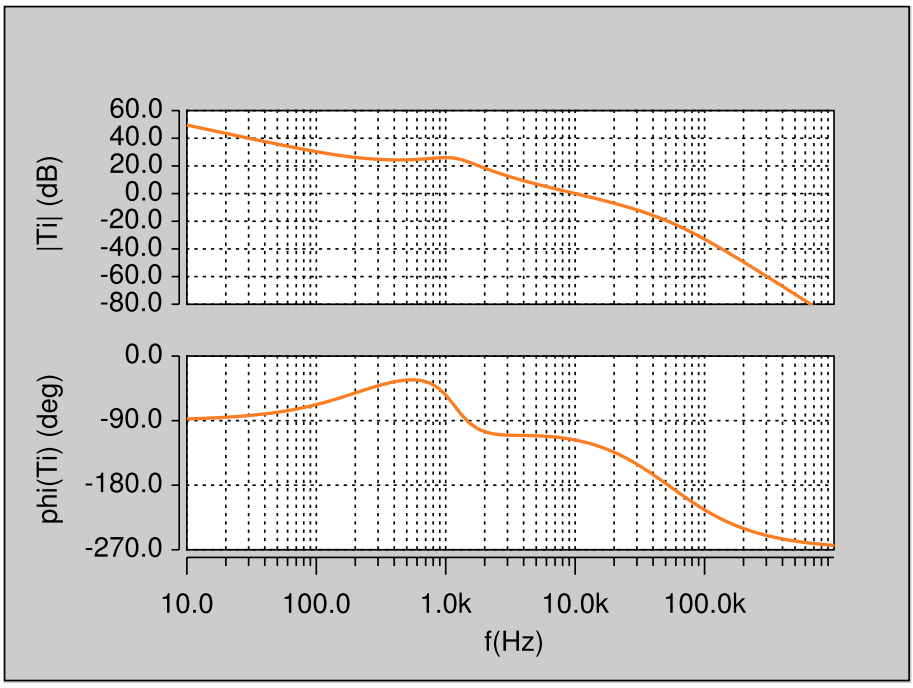

Figure 5.28: Magnitude and phase plots of compensated loop gain T_i of the inner-current loop obtained by circuit simulation.

5.6 Closed-Loop Transfer Functions for Inner-Current Loop

The following closed-loop control transfer functions are derived

- Reference voltage-to-inductor current transfer function T_{icl}.
- Reference voltage-to-output voltage transfer function T_{picl}.
- Input voltage-to-inductor current transfer function M_{icl}.
- Input voltage-to-output voltage transfer function M_{vicl}.
- Input voltage-to-duty cycle transfer function M_{di}.
- Input Impedance Z_{iicl}.
- Output Impedance Z_{oicl}.

5.6.1 Reference Voltage-to-Inductor Current Transfer Function T_{icl}

Using the block diagram shown in Fig. 5.29, the closed-loop reference voltage-to-inductor current transfer function is

$$T_{icl}(s) = \left.\frac{i_l(s)}{v_{ri}(s)}\right|_{v_i=i_o=0} = \frac{T_{ci}T_mT_{pi}}{1+T_i}. \tag{5.84}$$

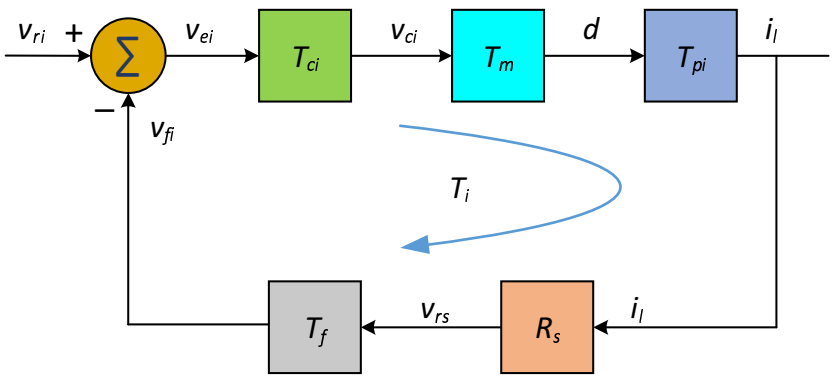

Figure 5.29: Block diagram used to derive inner-loop control-to-inductor current transfer function T_{icl}.

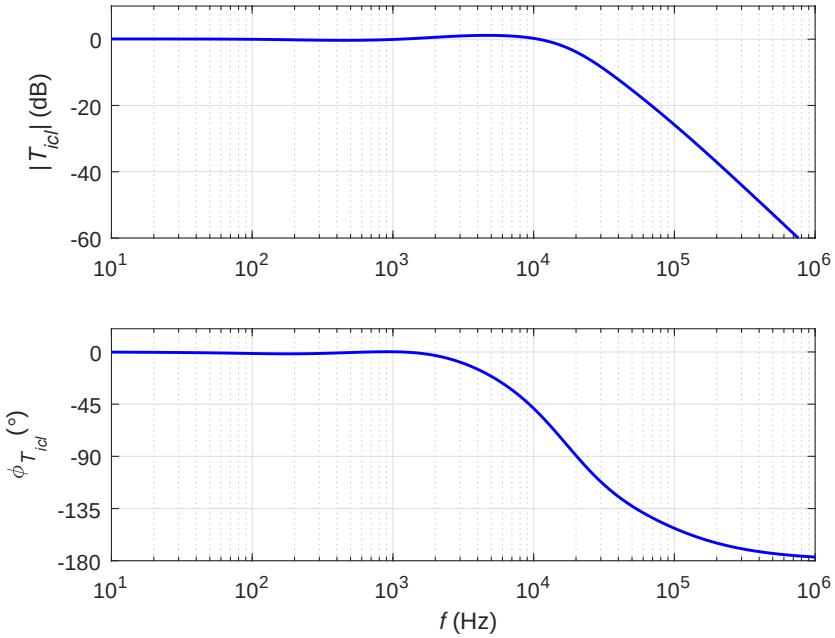

Figure 5.30: Theoretically obtained magnitude and phase plots of the inner-current loop reference voltage-to-inductor current transfer function T_{icl}.

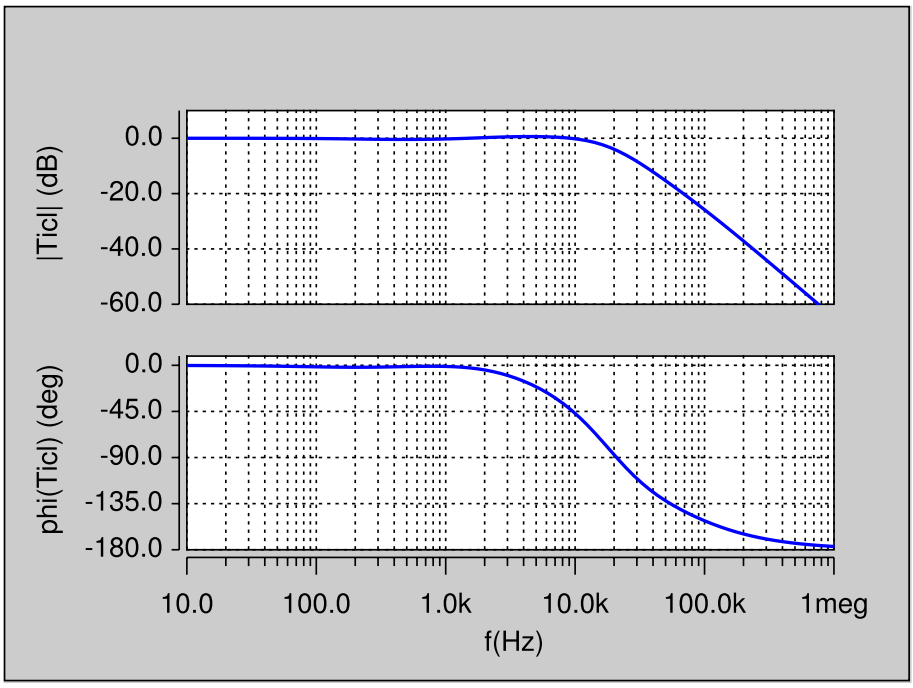

Figure 5.31: Magnitude and phase plots of the inner-current loop reference voltage-to-inductor current transfer function T_{icl} obtained by circuit simulation.

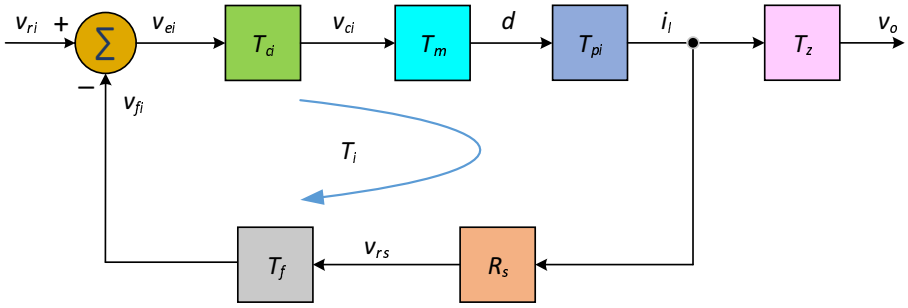

Figure 5.32: Block diagram required to derive inner-loop control-to-output voltage transfer function T_{picl}.

Fig. 5.30 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop reference voltage-to-inductor current transfer function. The theoretical results were validated by simulation. Fig. 5.31 shows the magnitude and phase plots of the inner-current loop reference voltage-to-inductor current transfer function using SABER Simulator.

5.6.2 Reference Voltage-to-Output Voltage Transfer Function T_{picl}

Using the block diagram shown in Fig. 5.32, the closed-loop reference voltage-to-output voltage transfer function is

$$T_{picl}(s) = \left.\frac{v_o(s)}{v_{ri}(s)}\right|_{v_i=i_o=0} = \frac{T_{ci}T_mT_{pi}T_z}{1+T_i}, \tag{5.85}$$

where T_z is the inductor current-to-output voltage transfer function given as

$$T_z(s) = \left.\frac{v_o(s)}{i_l(s)}\right|_{v_i=d=0} = Z_2 = R_L||\left(\frac{1}{sC}+r_C\right) \tag{5.86}$$

Fig. 5.33 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop reference voltage-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 5.34 shows the magnitude and phase plots of the inner-current loop reference voltage-to-output voltage transfer function using SABER Simulator.

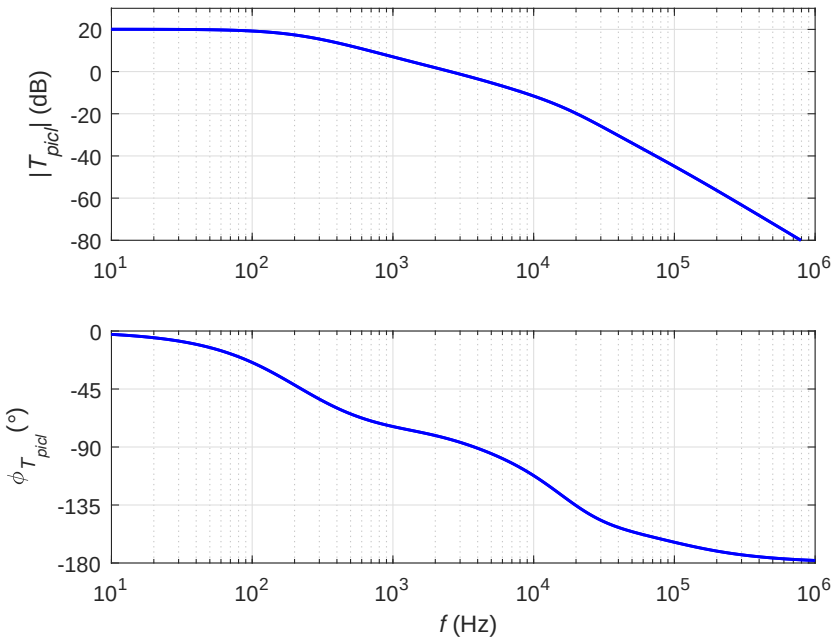

Figure 5.33: Theoretically obtained magnitude and phase plots of reference voltage-to-output voltage transfer function T_{picl}.

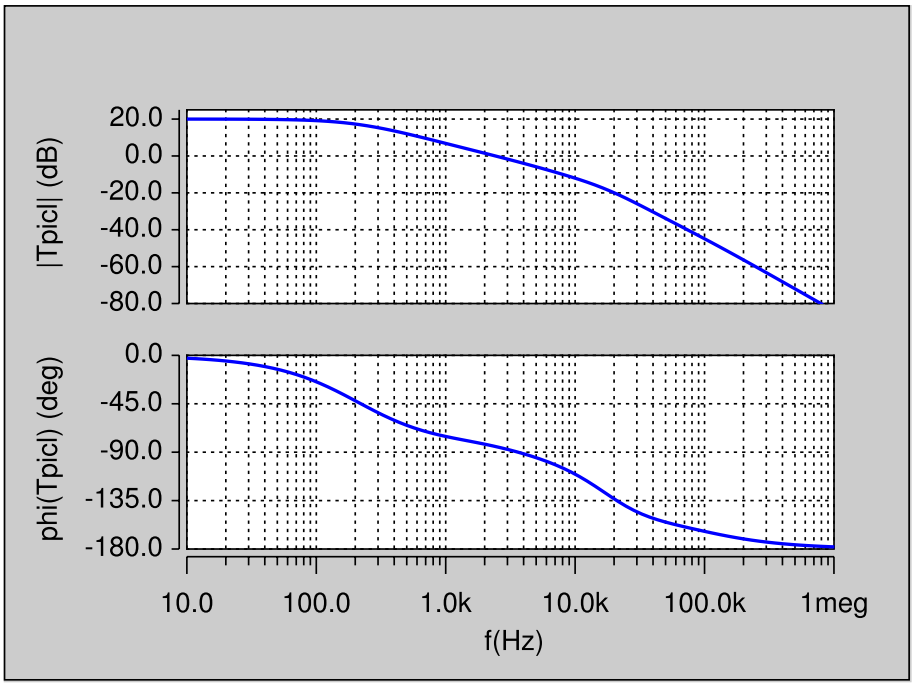

Figure 5.34: Magnitude and phase plots ofReference voltage-to-output voltage transfer function T_{picl} obtained by circuit simulation.

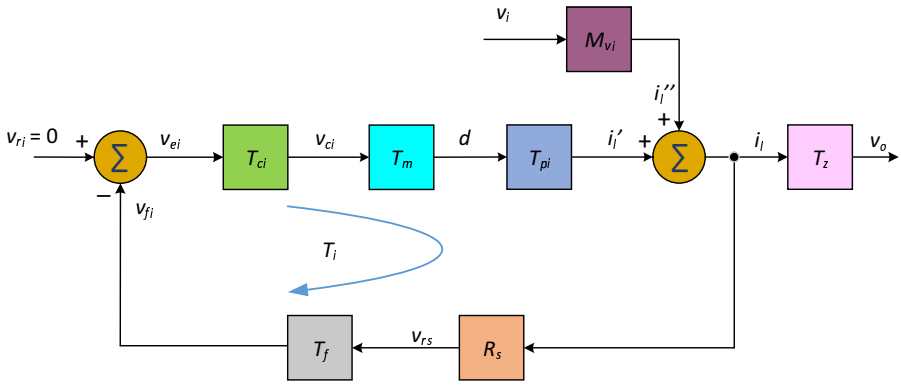

Figure 5.35: Block diagram required to derive inner-loop input voltage-to-inductor current transfer function M_{icl} and inner-loop input voltage-to-output voltage transfer function M_{vicl}.

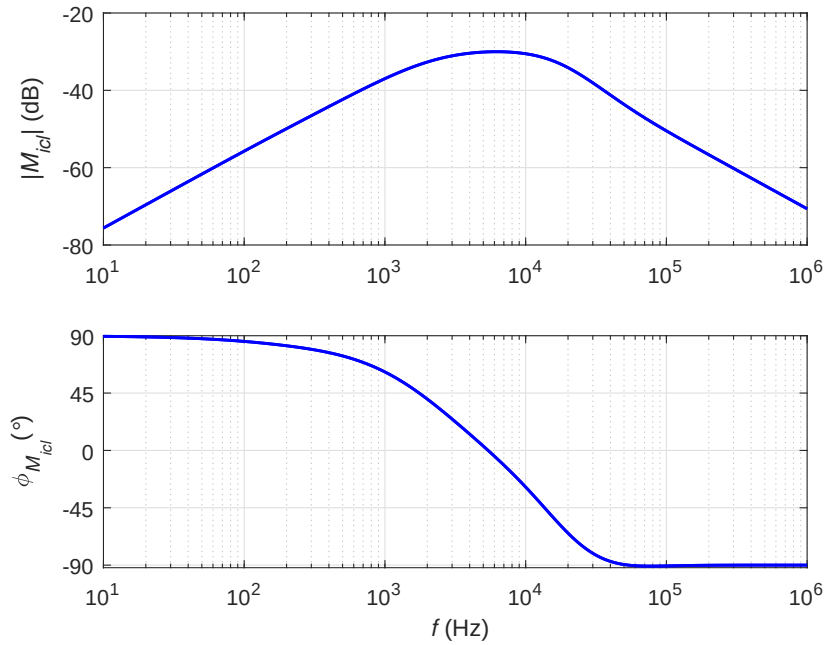

Figure 5.36: Theoretically obtained magnitude and phase plots of input voltage-to-inductor current transfer function M_{icl}.

5.6.3 Input Voltage-to-Inductor Current Transfer Function M_{icl}

Using the block diagram shown in Fig. , the closed-loop input voltage to inductor current transfer function is

$$M_{icl}(s) = \left.\frac{i_l(s)}{v_i(s)}\right|_{v_{ri}=i_o=0}. \tag{5.87}$$

From the block diagram

$$i_l = i_l' + i_l'' = -T_{ci}T_mT_{pi}T_fR_si_l + M_{vi}v_i = -T_ii_l + M_{vi}v_i. \tag{5.88}$$

$$i_l(1+T_i) = M_{vi}v_i. \tag{5.89}$$

Hence

$$M_{icl}(s) = \frac{i_l(s)}{v_i(s)} = \frac{M_{vi}}{1+T_i}. \tag{5.90}$$

Fig. 5.36 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop input voltage-to-inductor current transfer

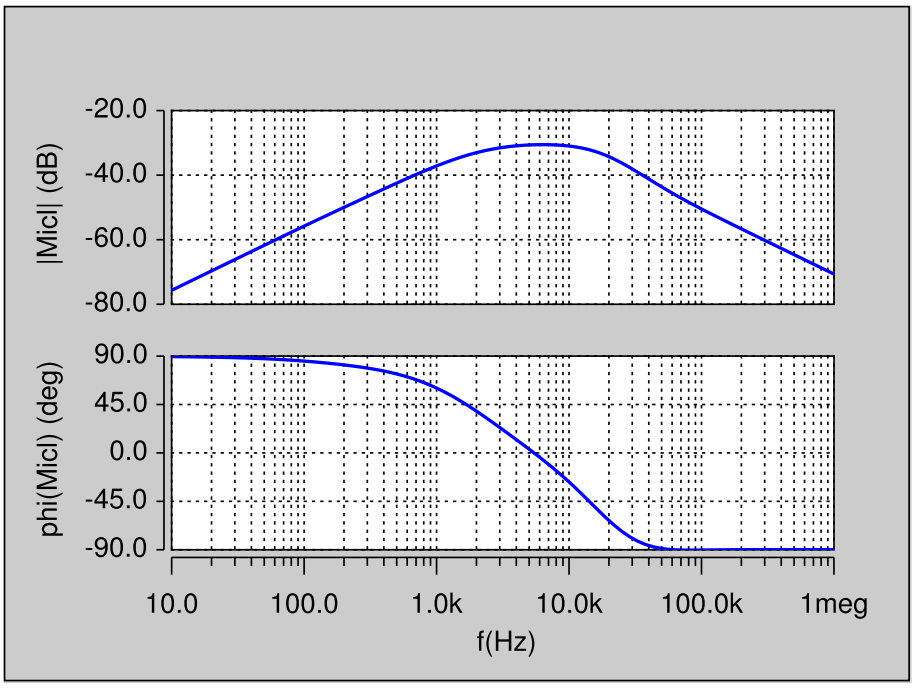

Figure 5.37: Magnitude and phase plots of input voltage-to-inductor current transfer function M_{icl} obtained by circuit simulation.

function. The theoretical results were validated by simulation. Fig. 5.37 shows the magnitude and phase plots of the inner-current loop input voltage-to-inductor current transfer function using SABER Simulator.

5.6.4 Input Voltage-to-Output Voltage Transfer Function M_{vicl}

Using the block diagram shown in Fig. 5.6.3, the closed-loop input voltage to output voltage transfer function is

$$M_{vicl}(s) = \left.\frac{v_o(s)}{v_i(s)}\right|_{v_{ri}=i_o=0}, \tag{5.91}$$

From (5.90), the closed-loop input-to-output transfer function is

$$M_{vicl}(s) = T_z M_{icl} = T_z \frac{M_{vi}}{1+T_i}. \tag{5.92}$$

Fig. 5.38 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop input voltage-to-output voltage transfer

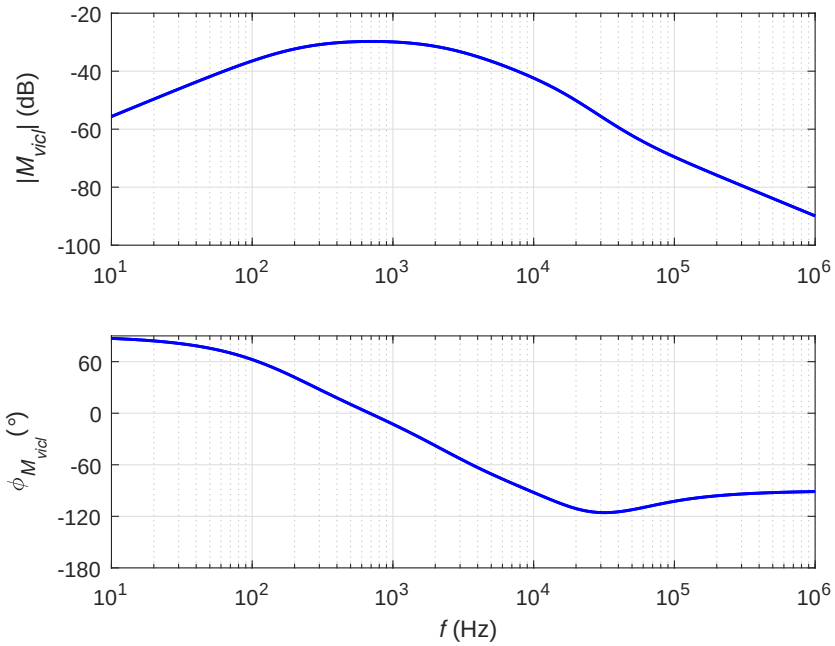

Figure 5.38: Theoretically obtained magnitude and phase plots of input voltage-to-output voltage transfer function transfer function M_{vicl}.

function. The theoretical results were validated by simulation. Fig. 5.39 shows the magnitude and phase plots of the inner-current loop input voltage-to-output voltage transfer function using SABER Simulator.

5.6.5 Input Impedance Z_{iicl}

The closed-inner-loop input impedance is

$$Z_{iicl}(s) = \left.\frac{v_i(s)}{i_i(s)}\right|_{i_o=d=0}. \tag{5.93}$$

From Fig. 5.40, the inductor current is

$$i_l = i_l' + i_l'' = T_{pi}d + M_{vi}v_i \tag{5.94}$$

and the duty cycle is

$$d = T_{ci}T_m v_{ei} = T_{ci}T_m(-T_f R_s i_l). \tag{5.95}$$

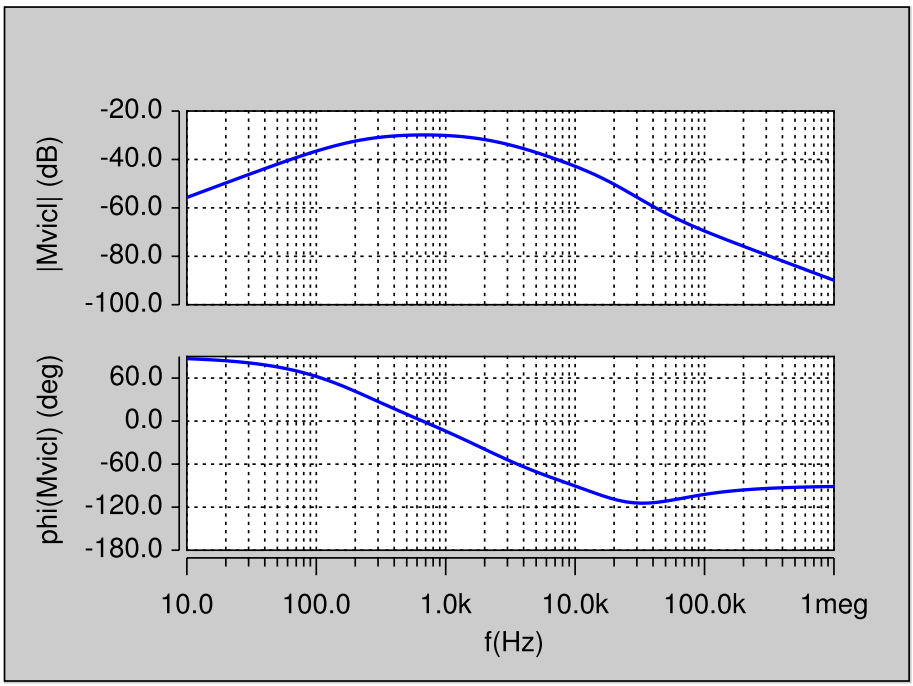

Figure 5.39: Magnitude and phase plots of input voltage-to-output voltage transfer function transfer function M_{vicl} obtained by circuit simulation.

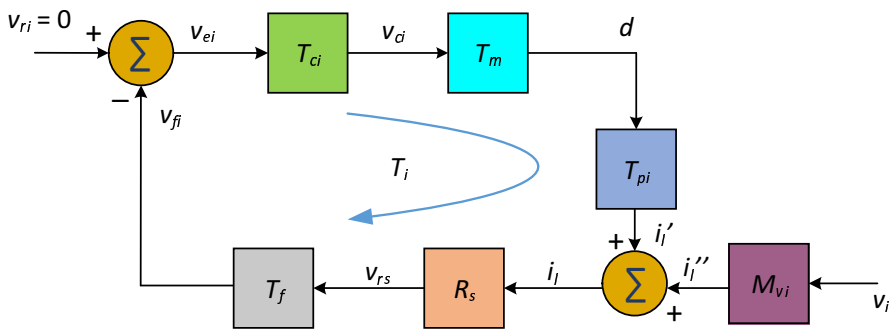

Figure 5.40: Block diagram used to derive inner-closed loop input impeance Z_{iicl}.

Substituting (5.95) in (5.94)

$$i_l = -T_{pi}T_{ci}T_mT_fR_si_l + M_{vi}v_i = -T_ii_l + M_{vi}v_i. \tag{5.96}$$

Rearranging (5.96)

$$i_l = \frac{M_{vi}}{1+T_i}v_i. \tag{5.97}$$

From (5.94),

$$d = \frac{i_l}{T_{pi}} - \frac{M_{vi}v_i}{T_{pi}}. \tag{5.98}$$

The input current is given as

$$\begin{aligned} i_i &= Di_l + I_Ld = Di_l + I_L\left(\frac{i_l}{T_{pi}} - \frac{M_{vi}v_i}{T_{pi}}\right) \\ &= \left(D + \frac{I_L}{T_{pi}}\right)i_l - \frac{M_{vi}I_L}{T_{pi}}v_i \\ &= \left[\left(D + \frac{I_L}{T_{pi}}\right)\frac{M_{vi}}{1+T_i} - \frac{M_{vi}I_L}{T_{pi}}\right]v_i. \end{aligned} \tag{5.99}$$

Hence, the closed-inner-loop input impedance is

$$Z_{iicl}(s) = \left.\frac{v_i(s)}{i_i(s)}\right|_{i_o=d=0} = \frac{T_{pi}(1+T_i)}{M_{vi}(DT_{pi} - I_LT_i)}. \tag{5.100}$$

The closed-loop input addmitance is

$$Y_{iicl}(s) = \frac{i_i(s)}{v_i(s)} = \frac{1}{Z_{iicl}(s)}. \tag{5.101}$$

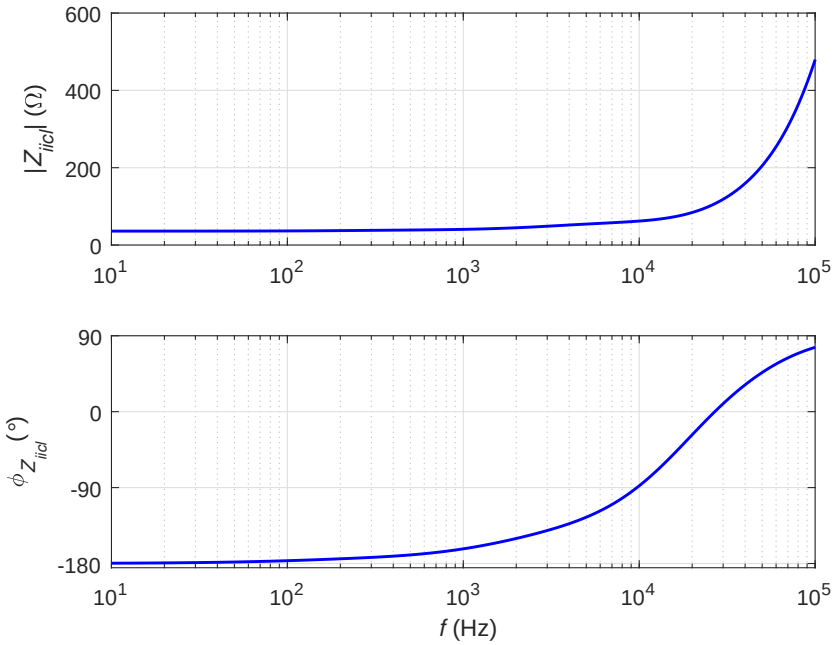

Figure 5.41: Theoretically obtained magnitude and phase plots of inner-loop input impedance Z_{iicl}.

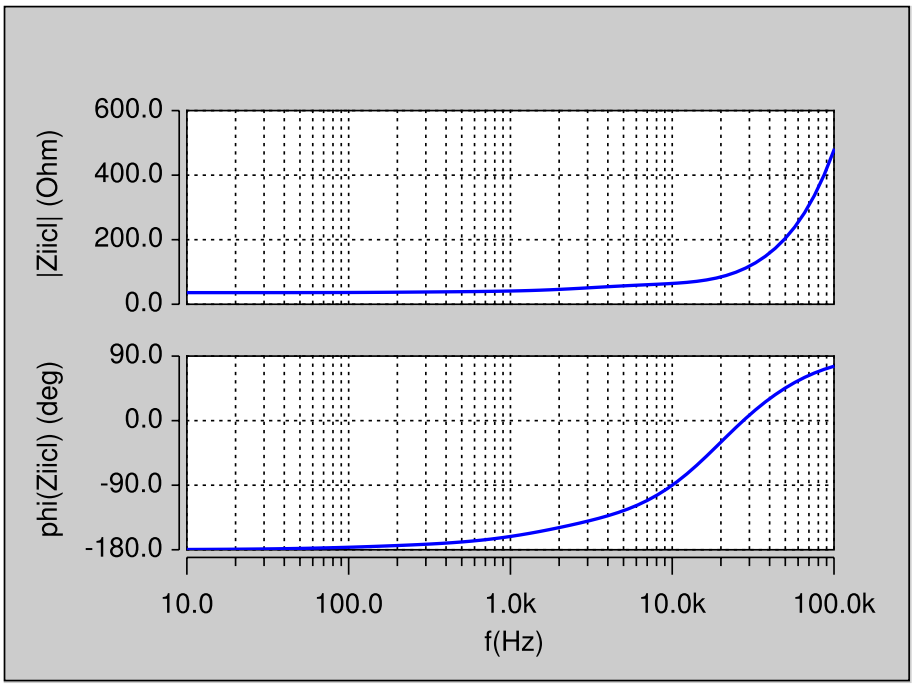

Figure 5.42: Magnitude and phase plots of inner-loop input impedance Z_{iicl} obtained by circuit simulation.

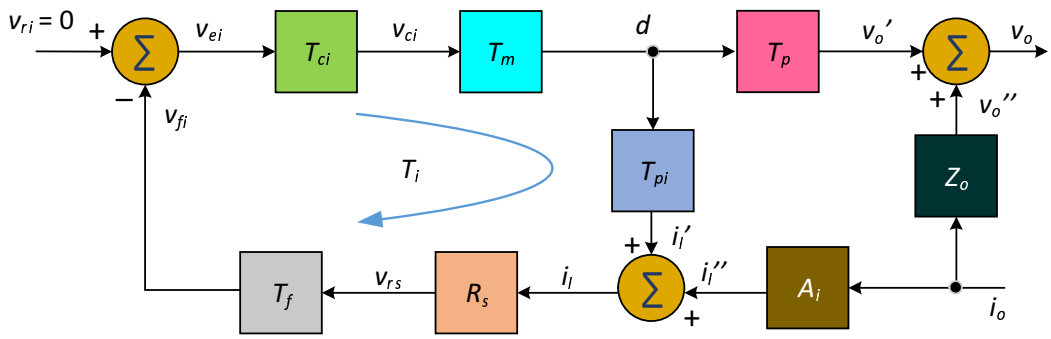

Figure 5.43: Block diagram required to derive inner-closed-loop input impedance Z_{oicl}.

Fig. 5.41 shows the theoretically obtained magnitude and phase plots of compensated loop gain of the inner-current loop input impedance. The theoretical results were validated by simulation. Fig. 5.42 shows the magnitude and phase plots of the inner-current loop input impedance using SABER Simulator.

5.6.6 Output Impedance Z_{oicl}.

Using the block diagram shown in Fig. 5.43, the closed-loop output impedance is

$$Z_{oicl}(s) = \left.\frac{v_o(s)}{i_o(s)}\right|_{v_{ri}=v_i=0}. \tag{5.102}$$

From the block diagram

$$i_l = i_l' + i_l'' = T_{pi}d + A_i i_o \tag{5.103}$$

and

$$\frac{-d}{T_{ix}} = T_{pi}d + A_i i_o \tag{5.104}$$

Rearranging

$$-d\left(\frac{1}{T_{ix}} + T_{pi}\right) = A_i i_o. \tag{5.105}$$

and

$$d = -\frac{A_i T_{ix}}{1 + T_i} i_o. \tag{5.106}$$

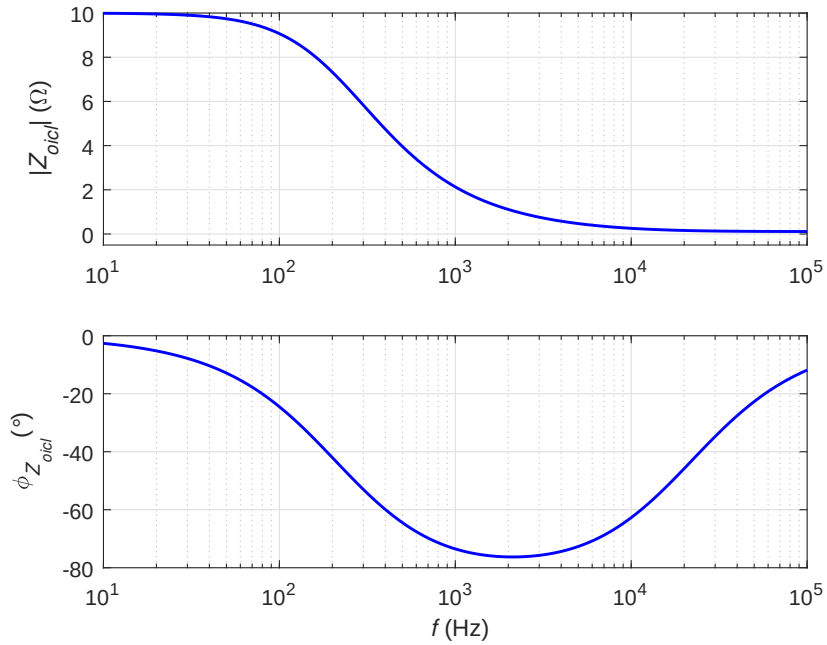

Figure 5.44: Theoretically obtained magnitude and phase plots of inner-closed loop output impedance Z_{oicl}.

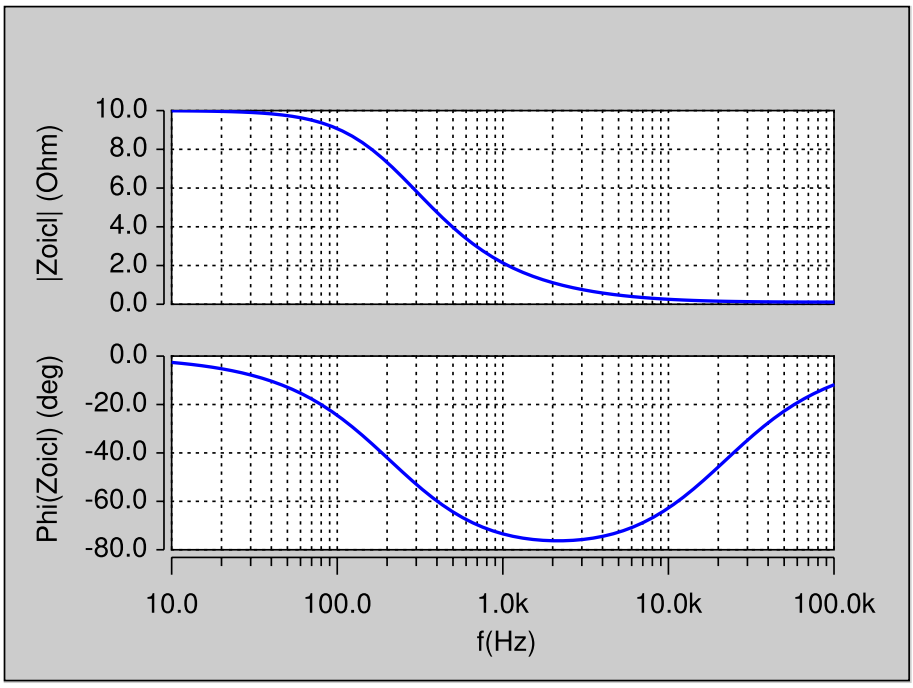

Figure 5.45: Magnitude and phase plots of inner-closed loop output impedance Z_{oicl} obtained by simulations.

From the block diagram in Fig. (5.43)

$$v_o = v_o' + v_o'' = T_p d + Z_o i_o. \tag{5.107}$$

Substituting d from (5.106), we get

$$v_o = T_p\left(- \frac{A_i T_{ix}}{1 + T_i} i_o \right) + Z_o i_o. = \left(Z_o - \frac{A_i T_p T_{ix}}{1 + T_i} \right) i_o. \tag{5.108}$$

The closed-loop output impedance is

$$Z_{oicl}(s) = \frac{v_o(s)}{i_o(s)} = Z_o - \frac{A_i T_p T_{ix}}{1 + T_i}. \tag{5.109}$$

Fig. 5.44 shows the theoretically obtained magnitude and phase plots of the inner-current loop output impedance. The theoretical results were validated by simulation. Fig. 5.45 shows the magnitude and phase plots of the inner-current loop output impedance using SABER Simulator.

5.7 Outer-Voltage Loop

5.7.1 Uncompensated Loop Gain for Outer-Voltage Loop T_{kv}

The natural behavior of the outer-voltage-loop can be determined using the uncompensated loop gain as

$$T_{kv} = \frac{v_{fv}}{v_{ev}} = \frac{\beta v_o}{v_{ri}} = \beta T_{picl}. \tag{5.110}$$

5.7.2 Transfer Function of Control Circuit for Outer-Voltage-Loop T_{cv}

An integral-single-lead control circuit introduces a pole at the origin required to boost the dc gain and a pole-zero pair to adjust crossover frequency f_c to maintain required PM. A detailed procedure to determine the transfer function of the controller to improve the dc gain ($>$ 50 dB) and achieve an inner current loop phase margin $PM = 60^\circ$ is explained in [34] and only the relevant expressions are presented here. The transfer function T_{ci} of the current loop control circuit is

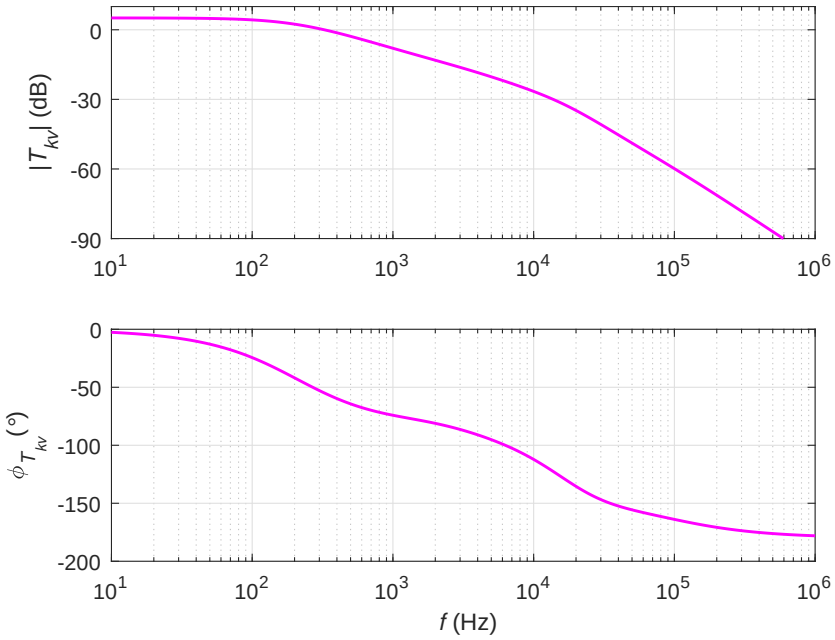

Figure 5.46: Theoretically obtained magnitude and phase plots of uncompensated loop gain T_{kv}.

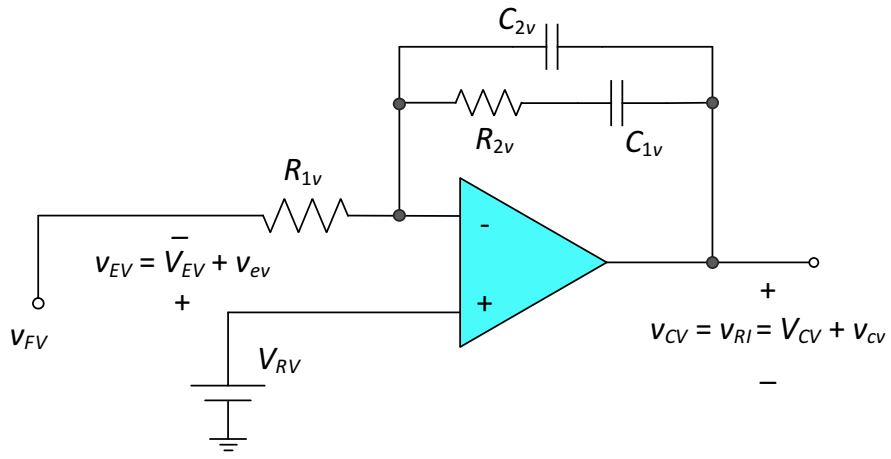

Figure 5.47: Circuit of type-II compensator used in outer-voltage loop.

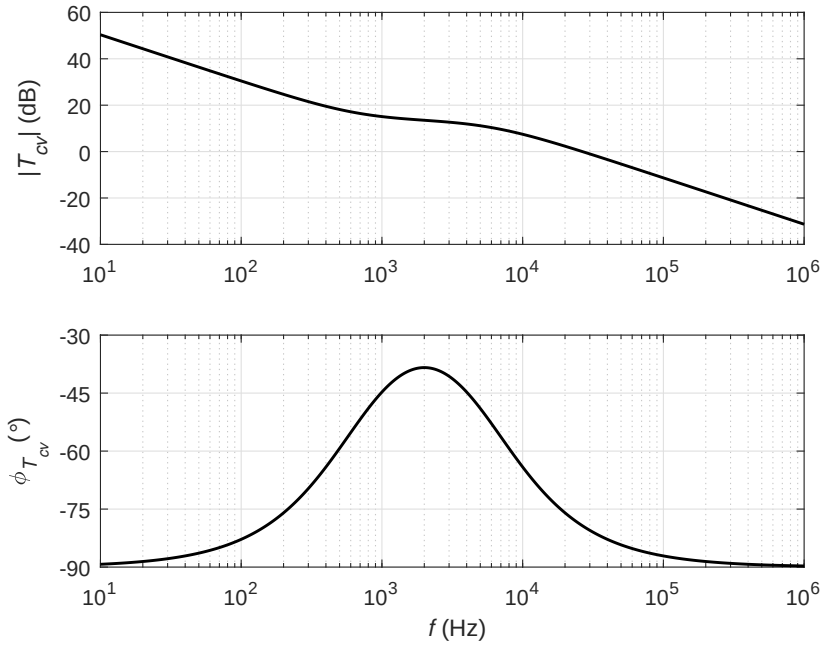

Figure 5.48: Theoretically obtained magnitude and phase plots of compensator transfer function T_{cv} for the outer-voltage loop.

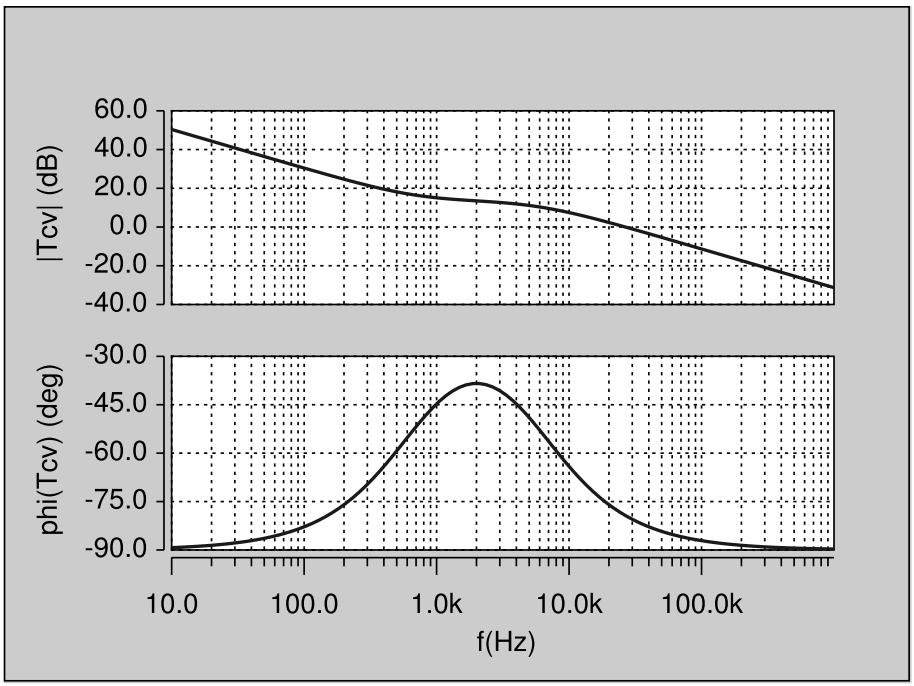

Figure 5.49: Magnitude and phase plots of the compensator transfer function T_{cv} for the outer-voltage loop obtained by circuit simulation.

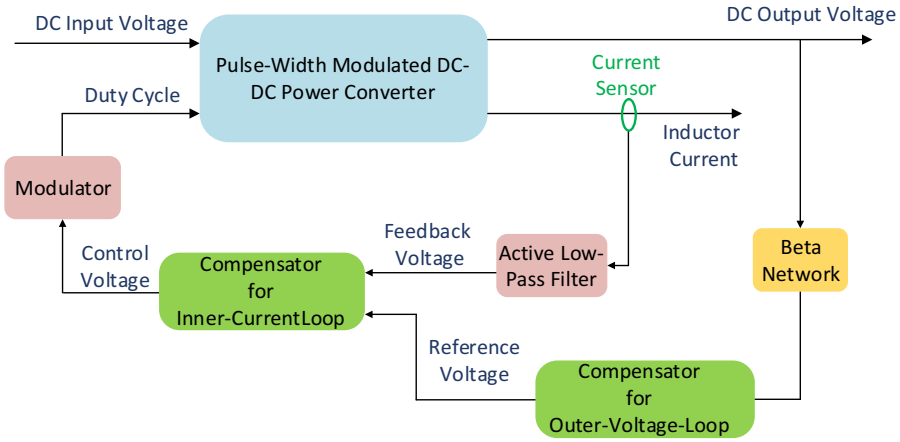

Figure 5.50: Architecture of true average current-mode control buck converter with outer-voltage loop.

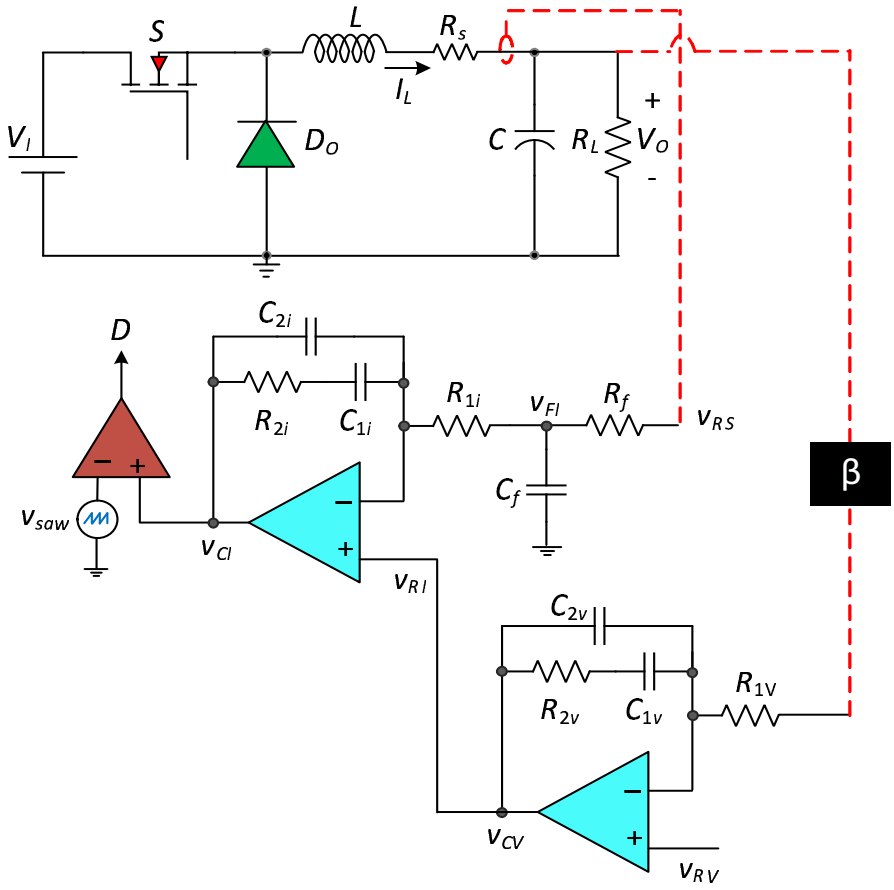

Figure 5.51: Circuit of average current-mode-control buck converter with outer-voltage loop.

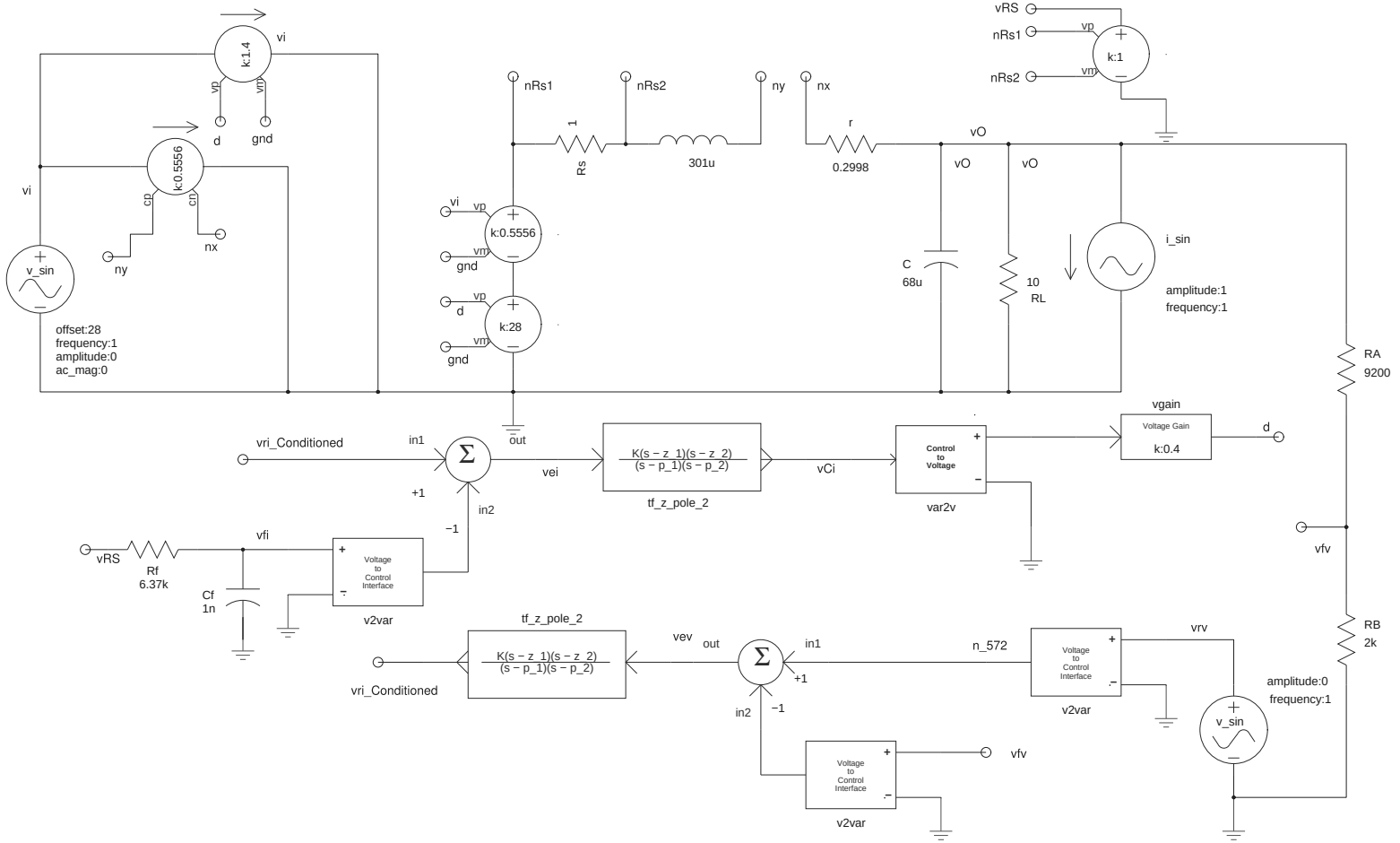

Figure 5.52: SABER schematic of small-signal model of true-average current-mode controlled buck converter with inner-current and outer-voltage loops.

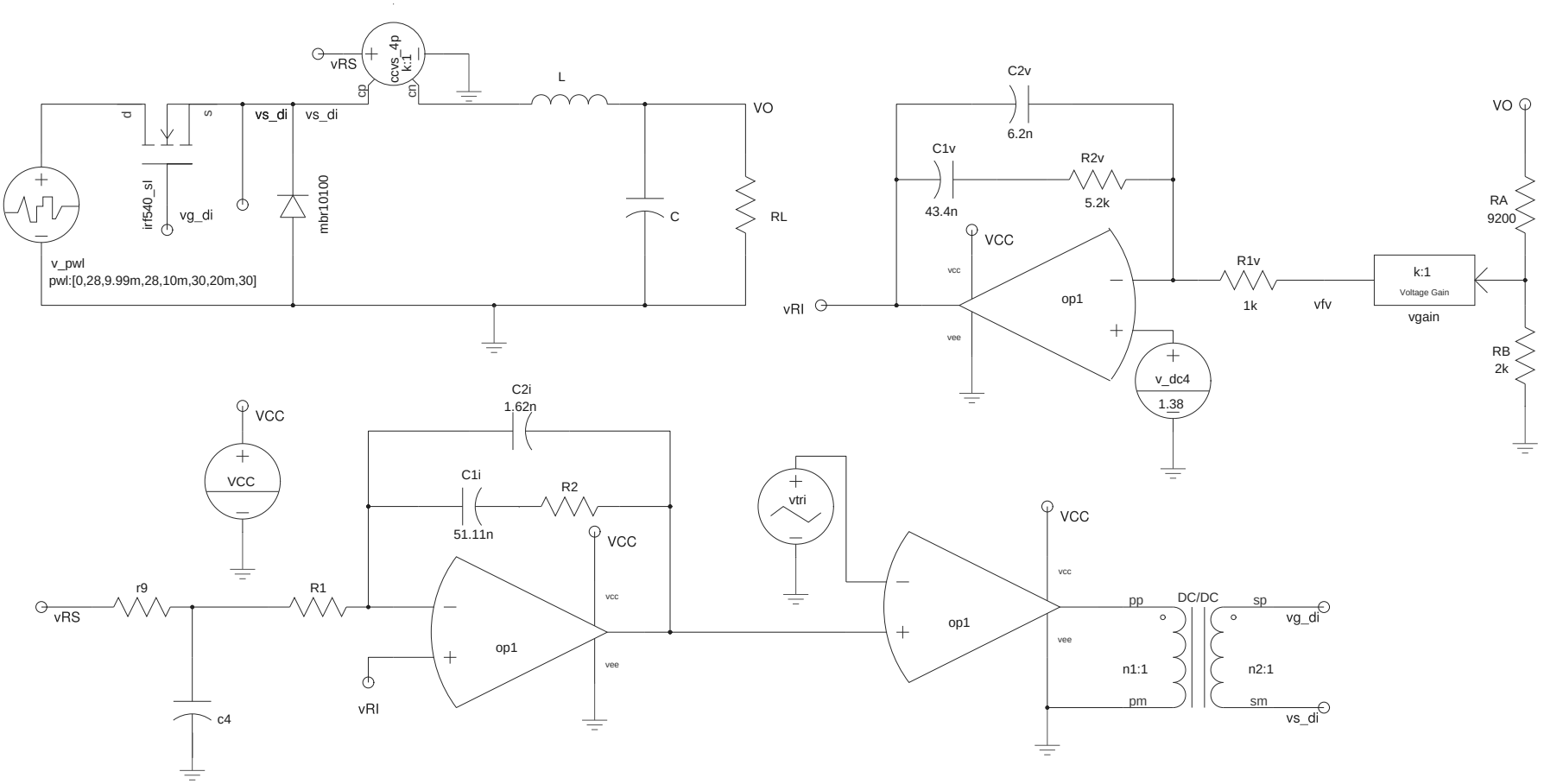

Figure 5.53: SABER schematic of true-average current-mode controlled buck converter with components.

$$T_{cv} = \frac{v_{cv}(s)}{v_{ev}(s)} = T_{cvo}\frac{1+\frac{s}{\omega_{zcv}}}{s\left(1+\frac{s}{\omega_{pcv}}\right)}, \tag{5.111}$$

where

$$T_{cvo} = \frac{1}{R_{1v}(C_{1v}+C_{2v})}, \tag{5.112}$$

$$\omega_{zcv} = \frac{1}{R_{2v}C_{1v}}, \tag{5.113}$$

and

$$\omega_{pcv} = \frac{C_{1v}+C_{2v}}{R_{2v}C_{1v}C_{2v}}. \tag{5.114}$$

Fig. 5.48 shows the theoretically obtained magnitude and phase plots of the compensator transfer function used in the outer-voltage loop. The theoretical results were validated by simulation. Fig. 5.49 shows the magnitude and phase plots of the compensator transfer function used in the outer-voltage loop using SABER Simulator.

5.7.3 Compensated Loop Gain of Outer Voltage-Loop T_v

The loop gain of the compensated inner-current loop is

$$T_v = \frac{v_{ev}}{v_{fv}} = T_{kv}T_{cv}, \tag{5.115}$$

to yield

$$T_v = T_{v0}\frac{(1+\frac{s}{\omega_{zi}})(1+\frac{s}{\omega_{zci}})}{s(1+\frac{s}{\omega_{pf}})(1+\frac{s}{\omega_{pci}})(1+\frac{2\xi s}{\omega_o}+\frac{s^2}{\omega_o^2})}, \tag{5.116}$$

where T_{v0} is the gain at $s=0$ given by

$$T_{v0} = T_{kv0}T_{cv0} = \frac{V_I R_s}{V_{Tm}(R_L+r)}\frac{1}{R_1(C_1+C_2)}. \tag{5.117}$$

Fig. 5.54 shows the theoretically obtained magnitude and phase plots of the loop gain of compensated outer-voltage loop. The theoretical results were validated by simulation. Fig. 5.55 shows the magnitude and phase plots of the loop gain of compensated outer-voltage loop using SABER Simulator.

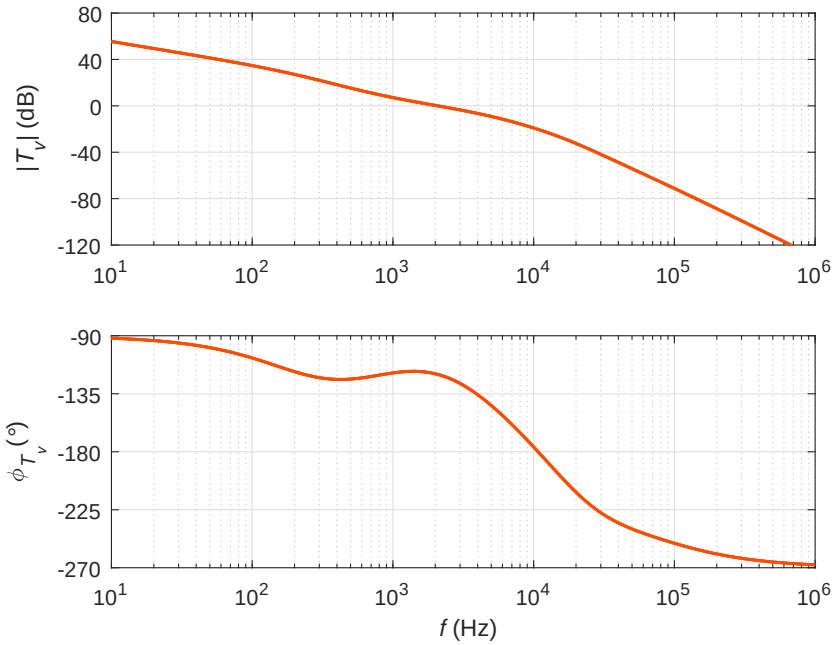

Figure 5.54: Theoretically obtained magnitude and phase plots of the loop gain T_v of the compensated outer-voltage loop.

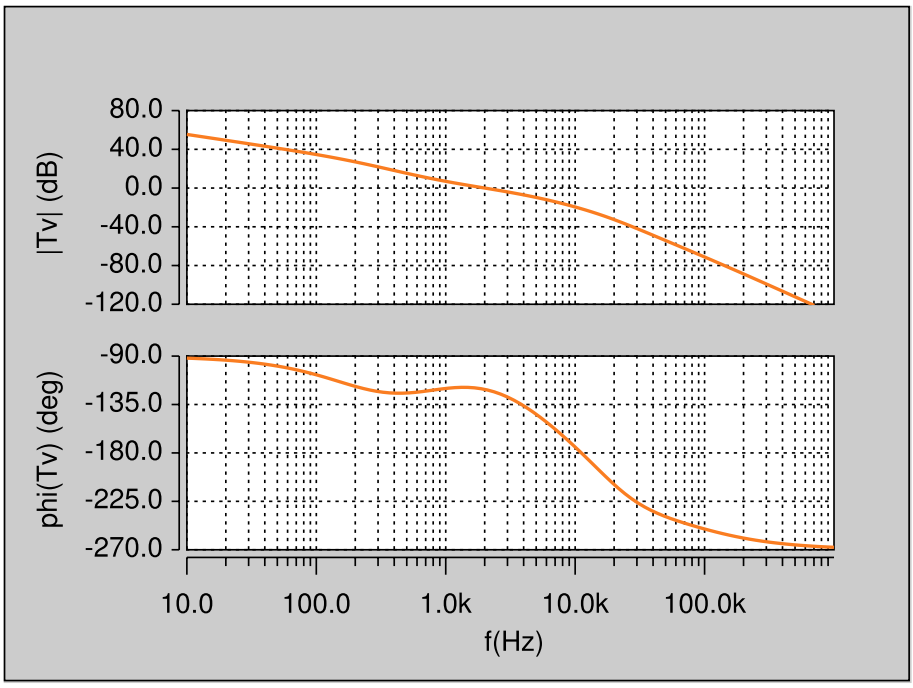

Figure 5.55: Magnitude and phase plots of the loop gain T_v of the compensated outer-voltage loop obtained by circuit simulation.

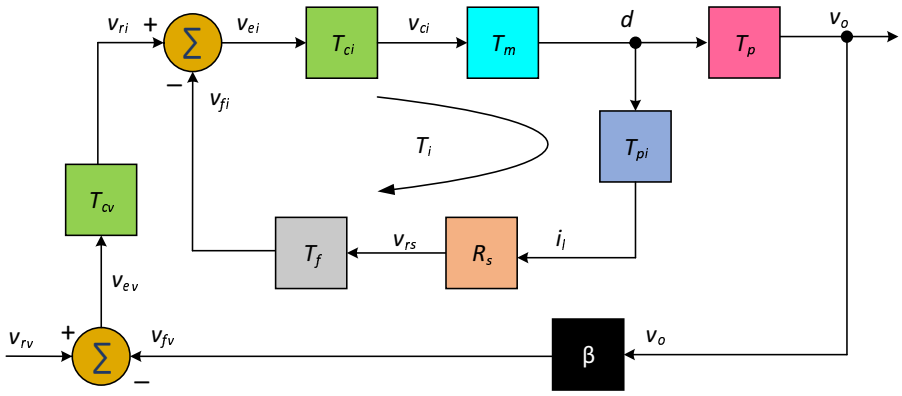

Figure 5.56: Block diagram used to derive control-to-output voltage transfer function T_{pcl}.

5.8 Closed-Loop Transfer Functions for Outer-Voltage Loop

The following closed-loop control transfer functions are derived

- Reference voltage-to-output voltage transfer function T_{pcl}
- Input voltage-to-output voltage transfer function M_{vcl}
- Input voltage-to-duty-cycle transfer function M_{dv}
- Input Impedance Z_{ivcl}.
- Output Impedance Z_{ovcl}.

5.8.1 Reference Voltage-to-Output Voltage Transfer Function T_{pcl}

Using the block diagram shown in Fig. 5.56, the closed-loop reference voltage-to-output voltage transfer function is

$$T_{pcl}(s) = \frac{v_o(s)}{v_{rv}(s)} = \frac{T_{cv}T_{picl}}{1+T_v}. \tag{5.118}$$

Fig. 5.57 shows the theoretically obtained magnitude and phase plots of the reference voltage-to-output voltage transfer function. The theoretical results were validated by simulation. Fig. 5.58 shows the magnitude and phase plots of the reference voltage-to-output voltage transfer function using SABER Simulator.

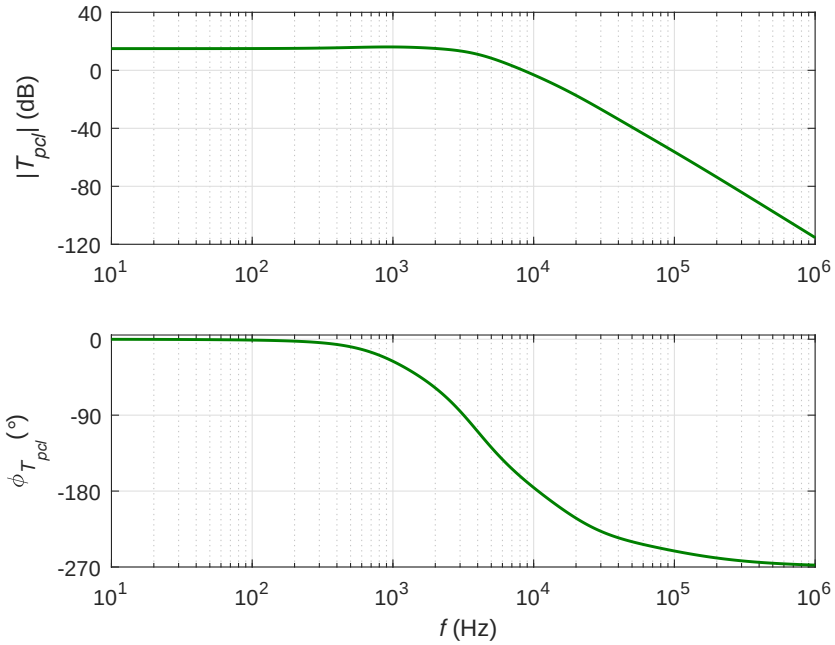

Figure 5.57: Theoretically obtained magnitude and phase plots of the reference voltage-to-output voltage transfer function T_{pcl}.

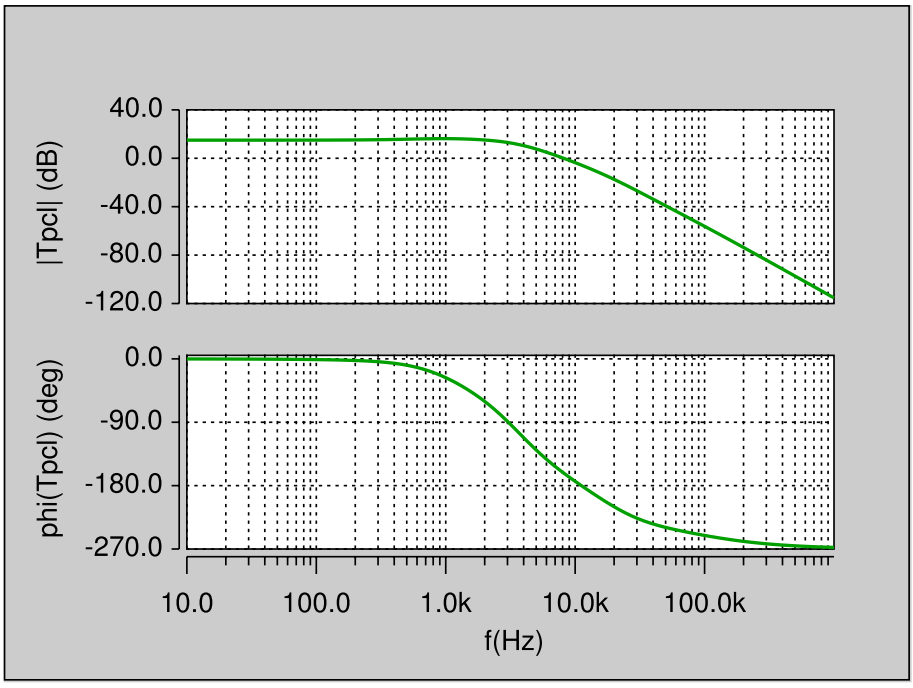

Figure 5.58: Magnitude and phase plots of the reference voltage-to-output voltage transfer function T_{pcl} obtained by circuit simulation.

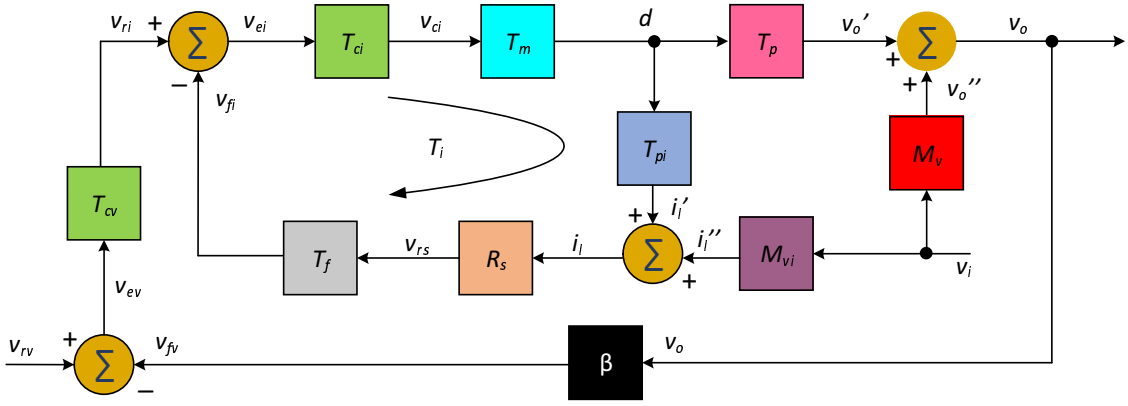

Figure 5.59: Block diagram used to derive the input voltage to duty-cycle transfer function M_{dv}.

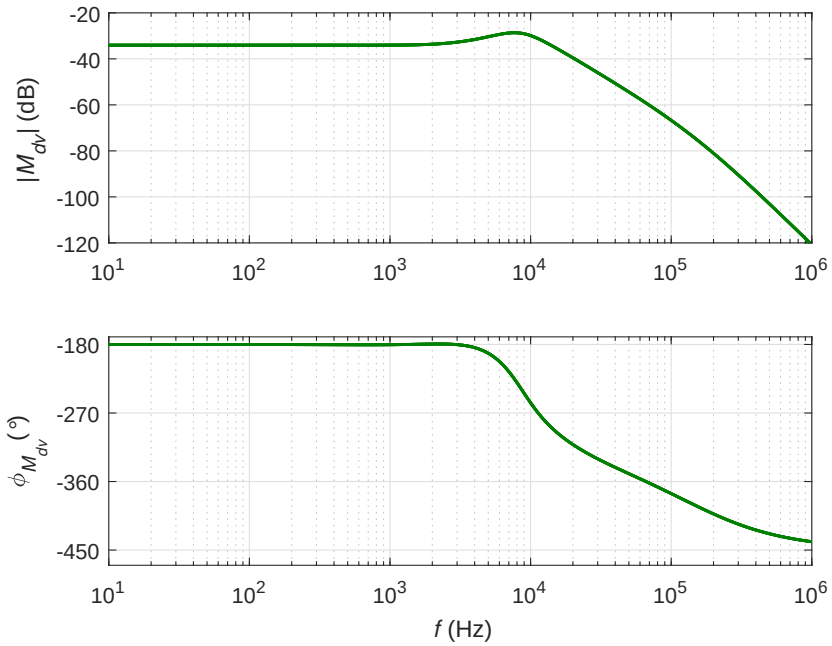

Figure 5.60: Theoretically obtained magnitude and phase plots of the input voltage-to-duty cycle transfer function M_{dv}.

5.8.2 Input voltage to duty-cycle transfer function M_{dv}

Using the block diagram shown in Fig. 5.59, the closed-loop input voltage to duty-cycle transfer function is

$$M_{dv}(s) = \frac{d(s)}{v_i(s)} \tag{5.119}$$

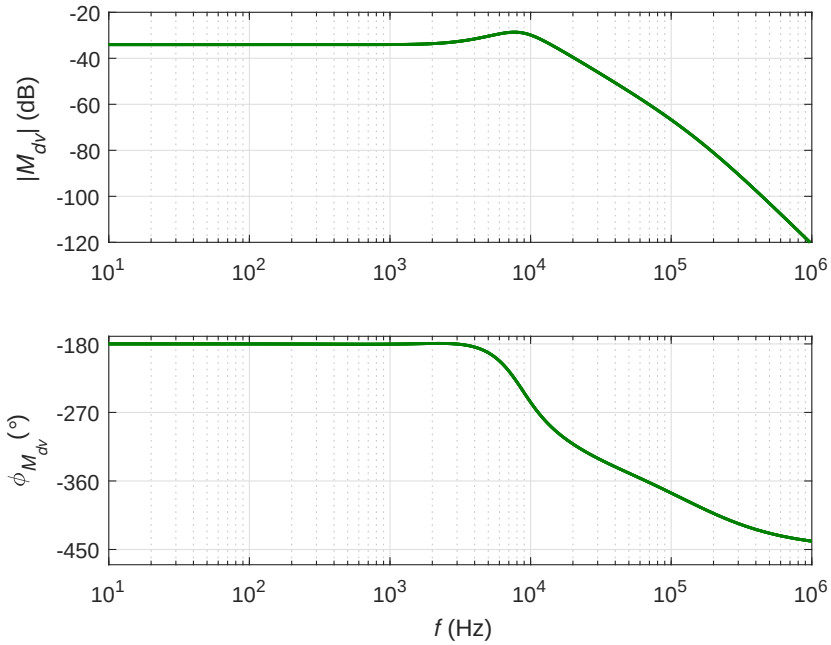

Figure 5.61: Magnitude and phase plots of the loop gain of the the input voltage-to-duty cycle transfer function M_{dv} obtained by circuit simulation.

From the block diagram

$$v_o = v_o' + v_o'' = T_p d + M_v v_i. \tag{5.120}$$

Also

$$v_{fv} = -\beta v_o \tag{5.121}$$

and

$$v_{cv} = v_{ri} = -\beta T_{cv} v_o. \tag{5.122}$$

The error voltage v_{ei} is

$$v_{ei} = v_{ri} - v_{fi} = -T_{cv}\beta v_o - R_s T_f i_l. \tag{5.123}$$

also

$$v_{ei} = \frac{d}{T_m T_{ci}}. \tag{5.124}$$

The inductor current is

$$i_l = T_{pi} d + M_{vi} v_i \tag{5.125}$$

Substituting (5.125) and (5.124) in (5.123), yeilds

$$\frac{d}{T_m T_{ci}} = -T_{cv}\beta v_o - R_s T_f (T_{pi} d + M_{vi} v_i). \tag{5.126}$$

Rearranging

$$v_o = -\frac{d}{T_{cv}\beta}\left(\frac{1}{T_m T_{ci}} + R_s T_f T_{pi}\right) - \frac{v_i}{T_{cv}\beta}\left(R_s T_f M_{vi}\right), \tag{5.127}$$

Equating (5.120) and (5.127) and rearranging

$$v_i\left(-\frac{M_{vi} R_s T_f}{T_{cv}\beta} - M_v\right) = d\left(T_p + \frac{1}{T_m T_{ci} T_{cv}\beta} + \frac{R_s T_f T_{pi}}{T_{cv}\beta}\right) \tag{5.128}$$

Equating (5.120) and (5.127) and rearranging

$$-\frac{v_i}{T_{cv}\beta}\left(M_{vi} R_s T_f + M_v T_{cv}\beta\right) = \frac{d}{T_{cv}\beta}\left(T_p T_{cv}\beta + \frac{1 + R_s T_f T_{pi} T_m T_{ci}}{T_m T_{ci}}\right). \tag{5.129}$$

Rearranging further

$$-v_i\left(M_{vi} R_s T_f + M_v T_{cv}\beta\right) = d\left(T_p T_{cv}\beta + \frac{1 + R_s T_f T_{pi} T_m T_{ci}}{T_m T_{ci}}\right) \tag{5.130}$$

and

$$M_{dv}(s) = \frac{d(s)}{v_i(s)} = -\frac{M_{vi} R_s T_f + \beta M_v T_{cv}}{\beta T_p T_{cv} + \dfrac{1 + T_i}{T_m T_{ci}}} \tag{5.131}$$

Fig. 5.60 shows the theoretically obtained magnitude and phase plots of the input voltage-to-duty cycle transfer function. The theoretical results were validated by simulation. Fig. 5.61 shows the magnitude and phase plots of the input voltage-to-duty cycle transfer function using SABER Simulator.

5.8.3 Input voltage to output voltage transfer function M_{vcl}

Using the block diagram shown in Fig. 5.62, the closed-loop input voltage to output voltage transfer function with outer-voltage-loop is

$$M_{vcl}(s) = \frac{v_o(s)}{v_i(s)}. \tag{5.132}$$

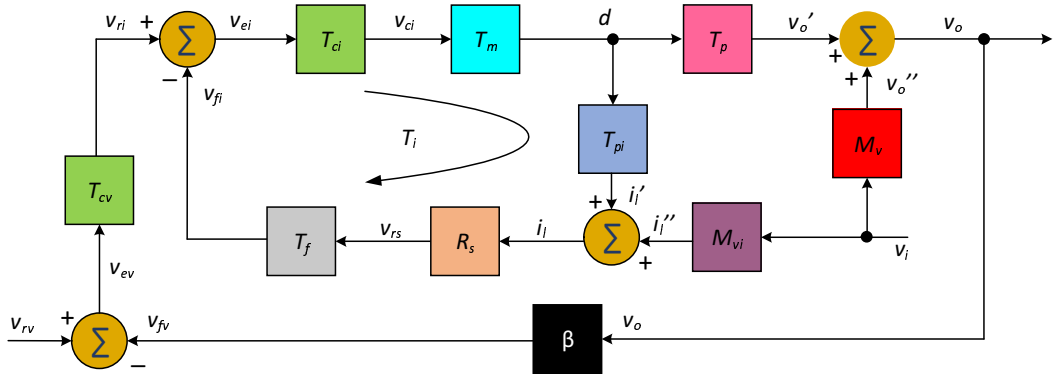

Figure 5.62: Block diagram used to derive the input voltage-to-output voltage transfer function M_{vcl}.

From (5.119)

$$d(s) = M_{dv} v_i(s). \tag{5.133}$$

Substituting (5.133) in

$$v_o = v_o' + v_o'' = T_p d + M_v v_i = T_p M_{dv} v_i + M_v v_i. \tag{5.134}$$

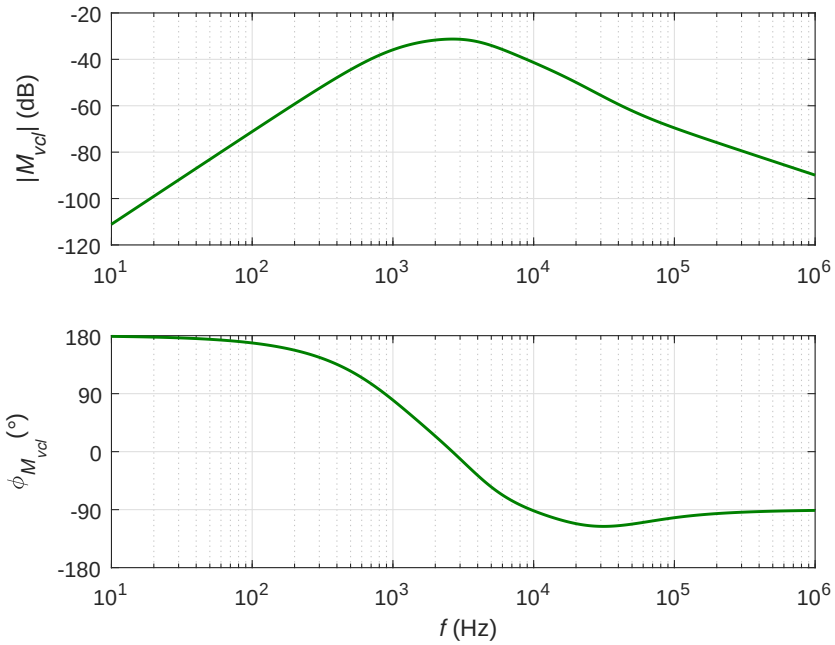

Figure 5.63: Theoretically obtained magnitude and phase plots of the input voltage-to-output voltage transfer function M_{vcl}.

Rearrangement of (5.134) yeilds

$$M_{vcl}(s) = \frac{v_o(s)}{v_i(s)} = T_p M_{dv} + M_v. \tag{5.135}$$

Fig. 5.63 shows the theoretically obtained magnitude and phase plots of the input voltage-to-output voltage transfer function M_{vcl}. The theoretical results were validated by simulation. Fig. 5.64 shows the magnitude and phase plots of the input voltage-to-output voltage transfer function M_{vcl} using SABER Simulator.

5.8.4 Input Impedance Z_{ivcl}

Using the block diagram shown in Fig. 5.65, the closed-loop input impedance with outer-voltage-loop is

$$Z_{ivcl}(s) = \frac{v_i(s)}{i_i(s)}. \tag{5.136}$$

From the Fig. 5.65,

$$v_o = v_o' + v_o'' = T_p d + M_v v_i \tag{5.137}$$

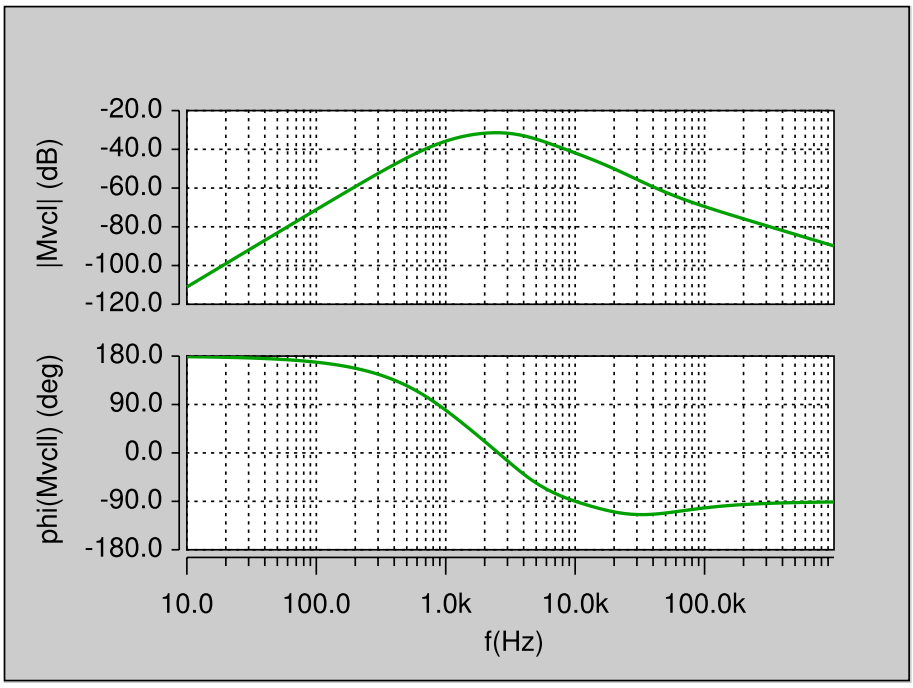

Figure 5.64: Magnitude and phase plots of the loop gain the input voltage-to-output voltage transfer function M_{vcl} obtained by circuit simulation.

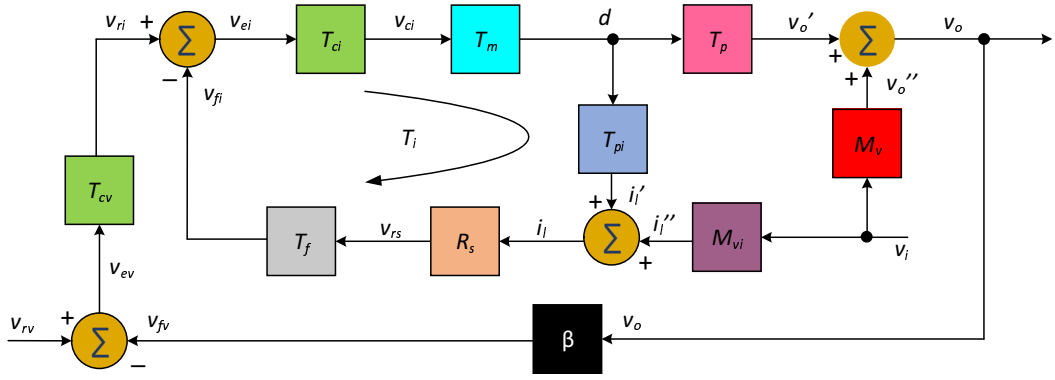

Figure 5.65: Block diagram used to derive the closed outer-voltage loop input impedance Z_{ivcl}.

and

$$i_l = i_l' + i_l'' = T_{pi}d + M_{vi}v_i. \tag{5.138}$$

Also

$$v_{fv} = \beta v_o, \tag{5.139}$$

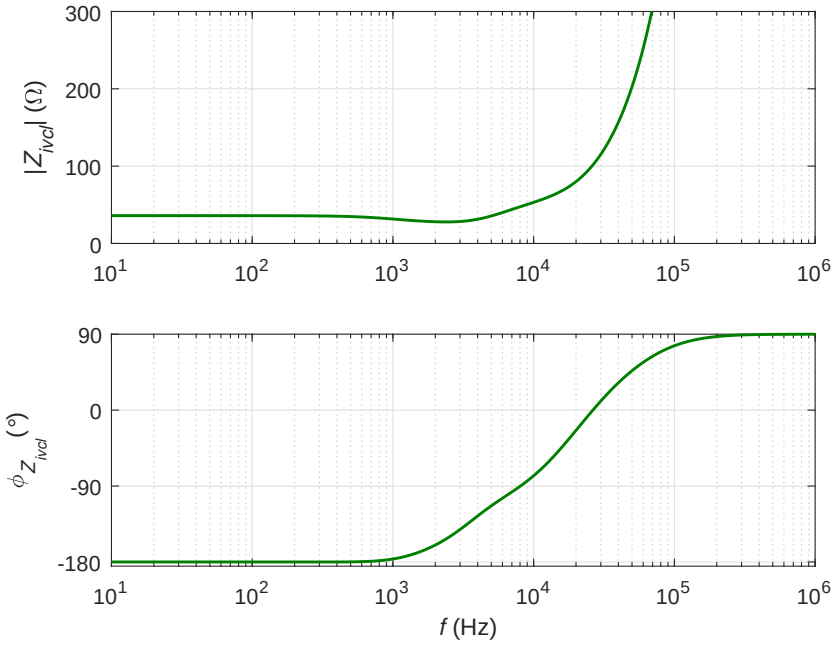

Figure 5.66: Theoretically obtained magnitude and phase plots of the closed outer-voltage loop input impedance Z_{ivcl}.

$$v_{ev} = v_{rv} - v_{fv} = 0 - \beta v_o = -\beta v_o \tag{5.140}$$

and

$$v_{cv} = v_{ri} = T_{cv} v_{ev} = -\beta T_{cv} v_o. \tag{5.141}$$

The error voltage v_{ei} is

$$v_{ei} = \frac{d}{T_{ci} T_m}. \tag{5.142}$$

The feedback voltage v_{fi} is

$$v_{fi} = T_f R_s i_l. \tag{5.143}$$

The reference voltage to inner-current-loop is

$$v_{ri} = v_{ei} + v_{fi}. \tag{5.144}$$

Substituting (5.141), (5.142) and (5.143) in (5.144)

$$-\beta T_{cv} v_o = \frac{d}{T_{ci} T_m} + T_f R_s i_l. \tag{5.145}$$

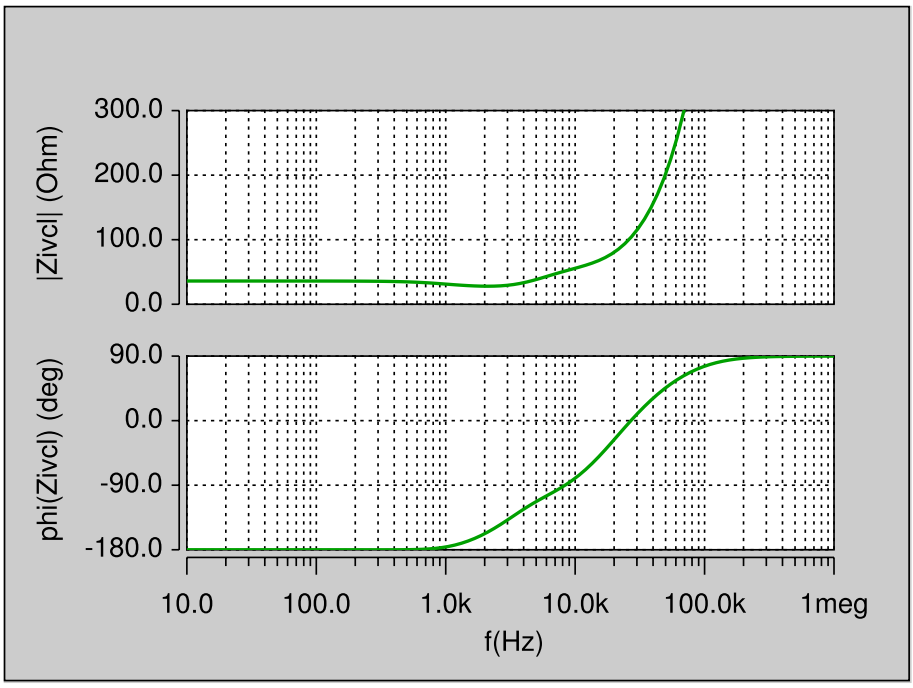

Figure 5.67: Magnitude and phase plots of the closed outer-voltage loop input impedance Z_{ivcl} obtained by circuit simulation.

Rearranging

$$v_o = -\frac{d}{\beta T_{cv} T_{ci} T_m} - \frac{T_f R_s i_l}{\beta T_{cv}}. \tag{5.146}$$

Substituting (5.137) in (5.146)

$$T_p d + M_v v_i = -\frac{d}{\beta T_{cv} T_{ci} T_m} - \frac{T_f R_s i_l}{\beta T_{cv}}. \tag{5.147}$$

Rearranging

$$d\left(T_p + \frac{1}{\beta T_{cv} T_{ci} T_m}\right) = -\frac{T_f R_s i_l}{\beta T_{cv}} - M_v v_i. \tag{5.148}$$

substituting (5.138) in (5.148)

$$d\left(T_p + \frac{1}{\beta T_{cv} T_{ci} T_m}\right) = -\frac{T_f R_s (T_{pi} d + M_{vi} v_i)}{\beta T_{cv}} - M_v v_i. \tag{5.149}$$

$$d\left(T_p + \frac{1}{\beta T_{cv} T_{ci} T_m} + \frac{T_f R_s T_{pi}}{\beta T_{cv}}\right) = \left(-\frac{T_f R_s M_{vi}}{\beta T_{cv}} - M_v\right). \tag{5.150}$$

$$d\left(\frac{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m}{\beta T_{ci} T_m T_{cv}}\right) = \left(\frac{-T_f R_s M_{vi} - \beta T_{cv} M_v}{\beta T_{cv}}\right). \tag{5.151}$$

$$d = -\frac{T_{ci} T_m (T_f R_s M_{vi} + \beta M_v T_{cv})}{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m} v_i \tag{5.152}$$

The input current i_i is

$$i_i = I_L d + D i_l = I_L d + D(T_{pi} d + M_{vi} v_i) = (I_L + D T_{pi}) d + D M_{vi} v_i. \tag{5.153}$$

substituting (5.152)

$$i_i = (I_L + D T_{pi}) \left[-\frac{T_{ci} T_m (T_f R_s M_{vi} + \beta M_v T_{cv})}{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m} v_i \right] + D M_{vi} v_i. \tag{5.154}$$

$$i_i = \left[-(I_L + D T_{pi}) \frac{T_{ci} T_m (T_f R_s M_{vi} + \beta M_v T_{cv})}{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m} + D M_{vi} \right] v_i \tag{5.155}$$

The closed-loop input admittance with outer-voltage-loop is

$$Y_{ivcl}(s) = \frac{i_i(s)}{v_i(s)} = -(I_L + D T_{pi}) \frac{T_{ci} T_m (T_f R_s M_{vi} + \beta M_v T_{cv})}{\beta T_p T_{ci} T_m T_{cv} + 1 + T_f R_s T_{pi} T_{ci} T_m} + D M_{vi} \tag{5.156}$$

The closed-loop input impedance with outer-voltage-loop is

$$Z_{ivcl}(s) = \frac{v_i(s)}{i_i(s)} = \frac{1}{Y_{ivcl}(s)}. \tag{5.157}$$

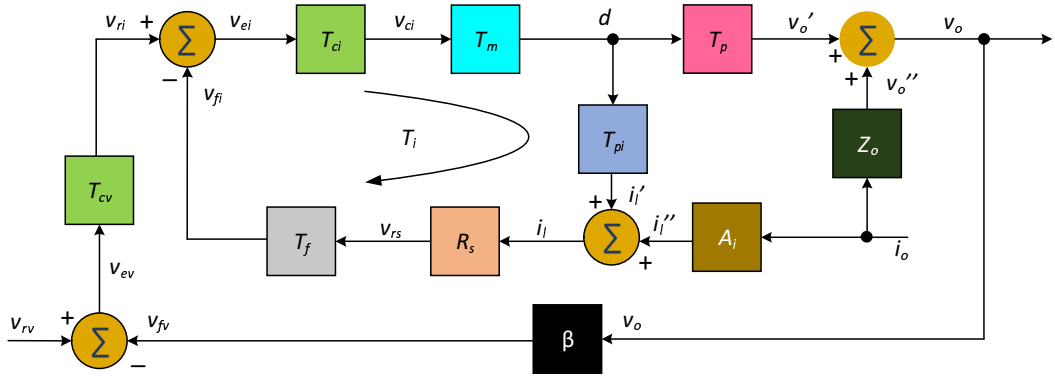

Figure 5.68: Block diagram used to derive the closed outer-voltage loop output impedance Z_{ovcl}.

Fig. 5.66 shows the theoretically obtained magnitude and phase plots of the closed-loop input impedance Z_{ivcl}. The theoretical results were validated by simulation. Fig. 5.67 shows the magnitude and phase plots of the closed-loop input impedance Z_{ivcl} using SABER Simulator.

5.8.5 Output Impedance Z_{ovcl}

Using the block diagram shown in Fig. 5.68, the closed-loop output impedance with outer-voltage-loop is

$$Z_{ovcl}(s) = \frac{v_o(s)}{i_o(s)}. \tag{5.158}$$

From the Fig. 5.68,

$$v_o = v_o' + v_o'' = T_p d + Z_o i_o. \tag{5.159}$$

and

$$i_l = i_l' + i_l'' = A_i i_o + T_{pi} d. \tag{5.160}$$

Also

$$v_{fv} = \beta v_o \tag{5.161}$$

and

$$v_{cv} = v_{ri} = -\beta T_{cv} v_o. \tag{5.162}$$

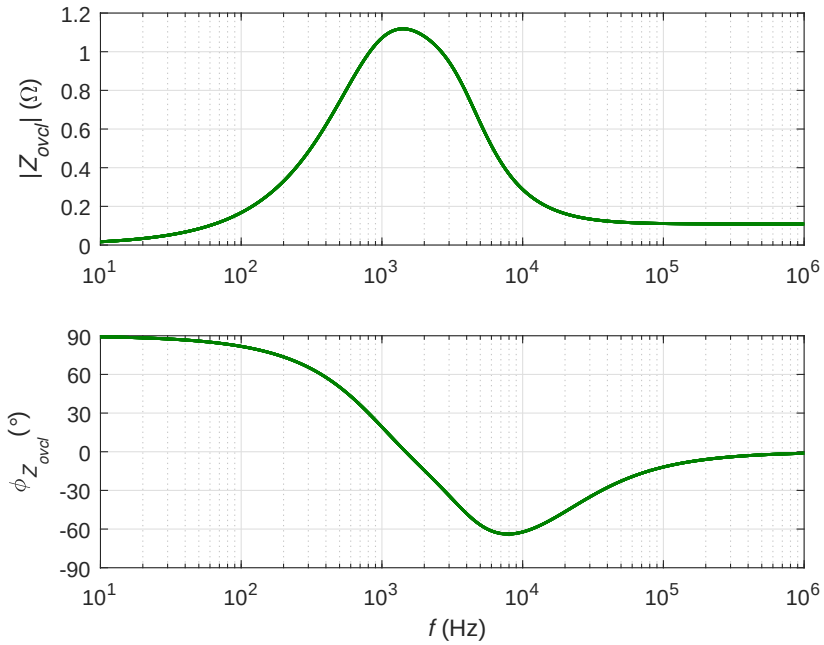

Figure 5.69: Theoretically obtained magnitude and phase plots of the closed outer-voltage loop output impedance Z_{ovcl}.

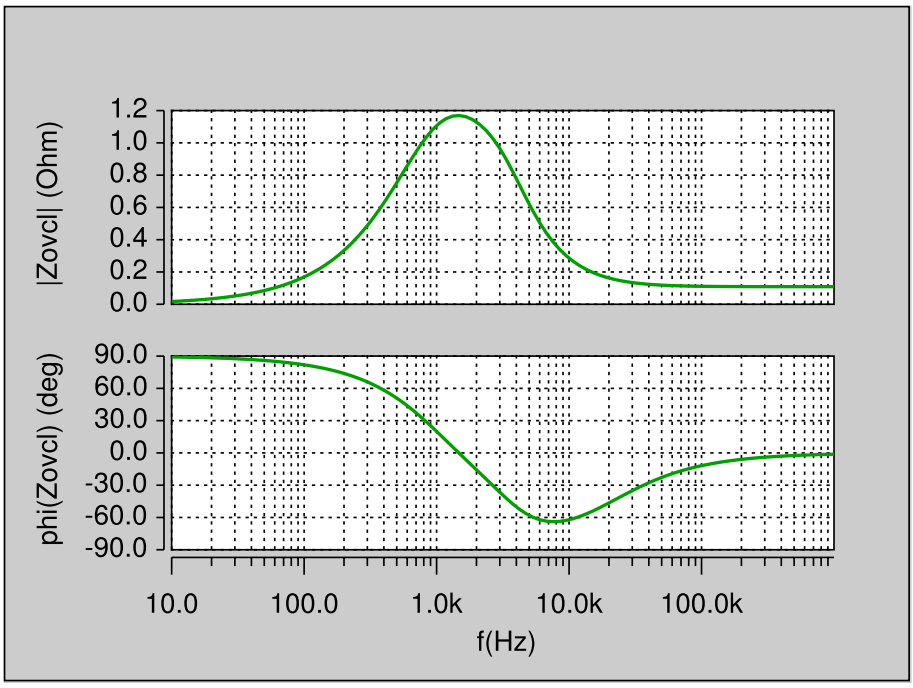

Figure 5.70: Magnitude and phase plots of the closed outer-voltage loop output impedance Z_{ovcl} obtained by circuit simulation.

The error voltage v_{ei} is

$$v_{ei} = v_{ri} - v_{fi} = -T_{cv}\beta v_o - R_s T_f i_l. \tag{5.163}$$

and

$$v_{ei} = \frac{d}{T_m T_{ci}}. \tag{5.164}$$

Substituting (5.160) and (5.164) in (5.163), yields

$$\frac{d}{T_m T_{ci}} = -T_{cv}\beta v_o - R_s T_f (A_i i_o + T_{pi} d.). \tag{5.165}$$

Rearranging (5.165)

$$d = -\frac{(T_{cv}\beta v_o + R_s T_f A_i i_o) T_{ci} T_m}{1 + T_i} \tag{5.166}$$

Substituting (5.166) in (5.159), yields

$$v_o = T_p \left[-\frac{(T_{cv}\beta v_o + R_s T_f A_i i_o) T_{ci} T_m}{1 + T_i} \right] + Z_o i_o. \tag{5.167}$$

Rearranging

$$v_o \left(1 + \frac{\beta T_p T_{cv} T_{ci} T_m}{1 + T_i} \right) = i_o \left(Z_o - \frac{T_p R_s T_f A_i T_{ci} T_m}{1 + T_i} \right) \tag{5.168}$$

Hence the closed-loop output impedance with outer-voltage-loop is

$$Z_{ovcl}(s) = \frac{v_o(s)}{i_o(s)} = \frac{Z_o(1 + T_i) - A_i T_p T_{ix}}{1 + T_i + T_p T_{cv} \beta T_{ci} T_m}. \tag{5.169}$$

Fig. 5.69 shows the theoretically obtained magnitude and phase plots of the closed-loop output impedance Z_{ovcl}. The theoretical results were validated by simulation. Fig. 5.70 shows the magnitude and phase plots of the closed-loop output impedance Z_{ovcl} using SABER Simulator.

5.9 Results

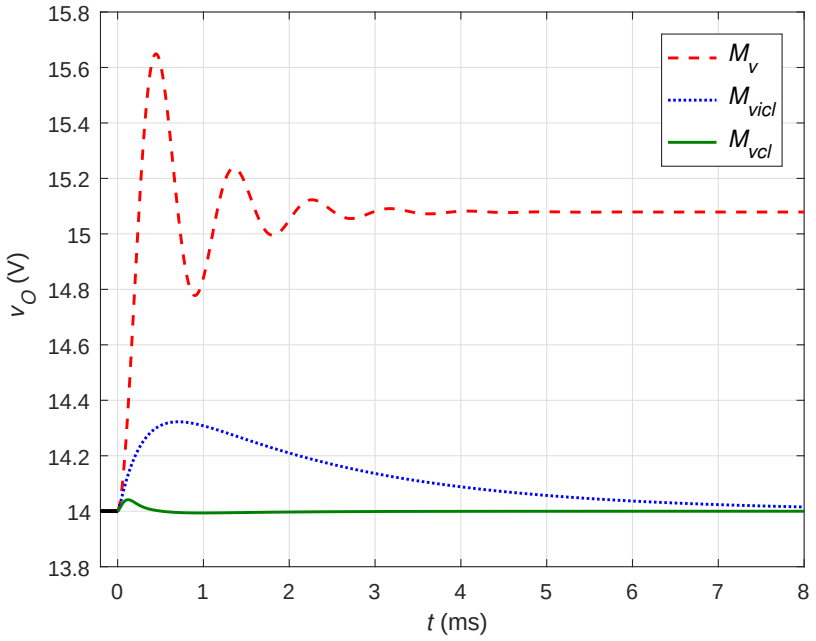

Figure 5.71: Comparison of responses in output voltages for step changes in input voltage by 1 V obtained using M_v, M_{vicl}, and M_{vcl} transfer functions, respectively.

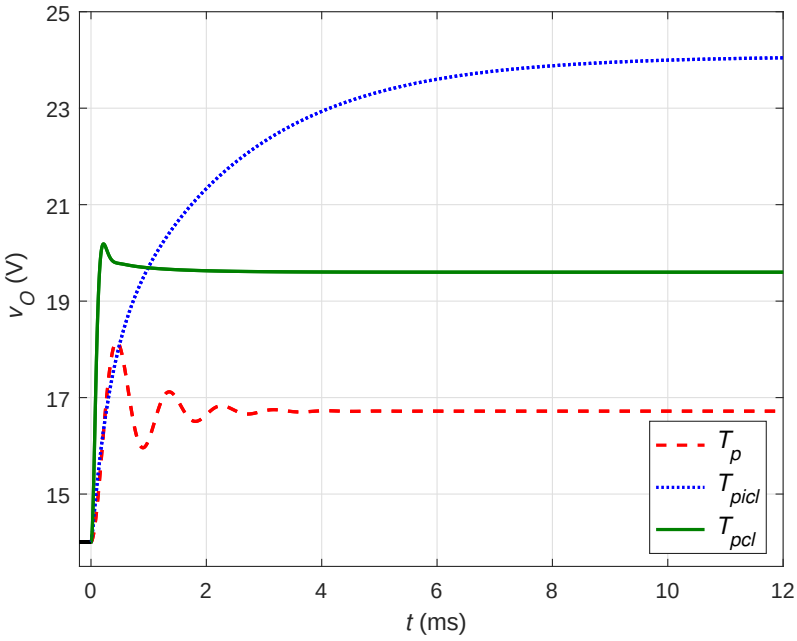

Figure 5.72: Comparison of responses in output voltages for step changes in duty cycle, current-loop reference, and voltage-loop reference voltages obtained using T_p, T_{picl}, and T_{pcl} transfer functions, respectively.

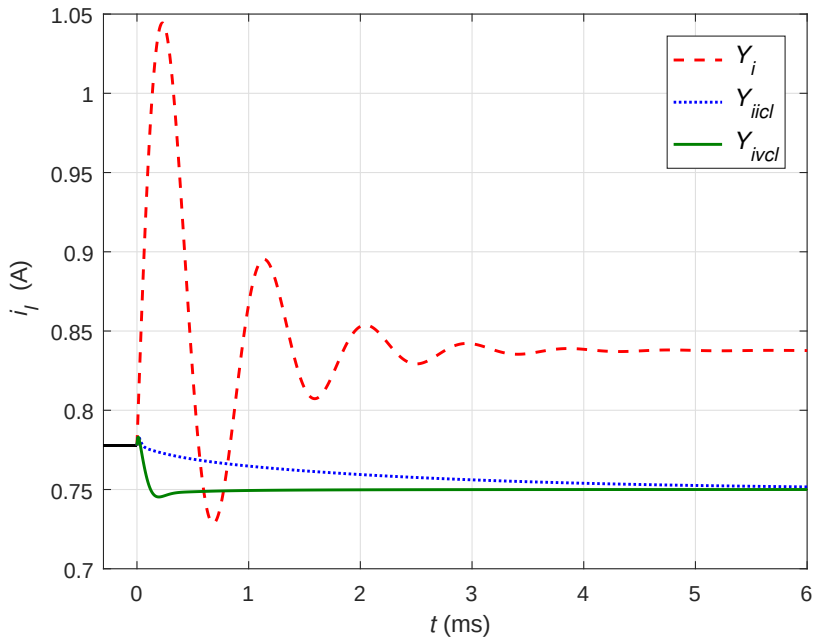

Figure 5.73: Comparison of the responses in input current for step change in the input voltage for the open-loop, power stage with only closed-inner loop, and with two-loop controlled buck dc-dc converter.

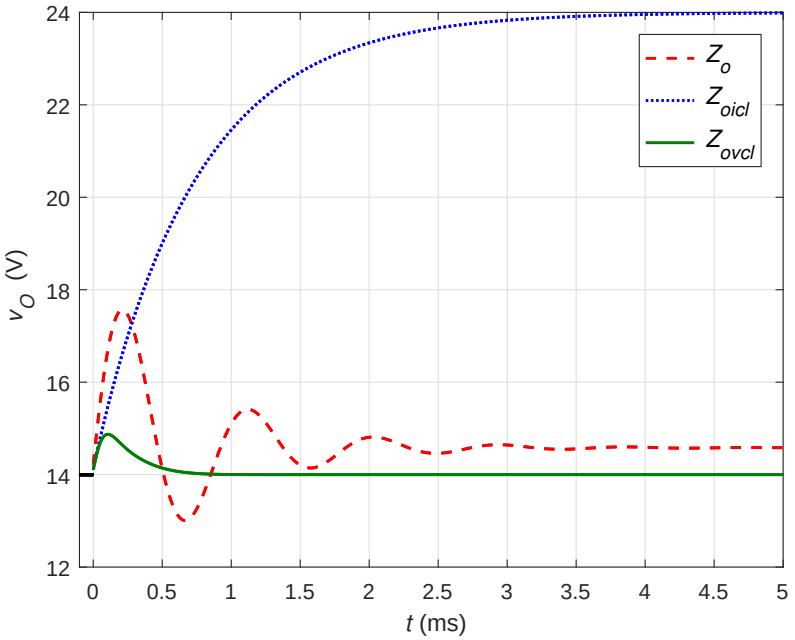

Figure 5.74: Comparison of responses in the output voltage for step changes in the load current by 1 A for the open-loop, power stage with only closed-inner loop, and with two-loop controlled buck dc-dc converter.

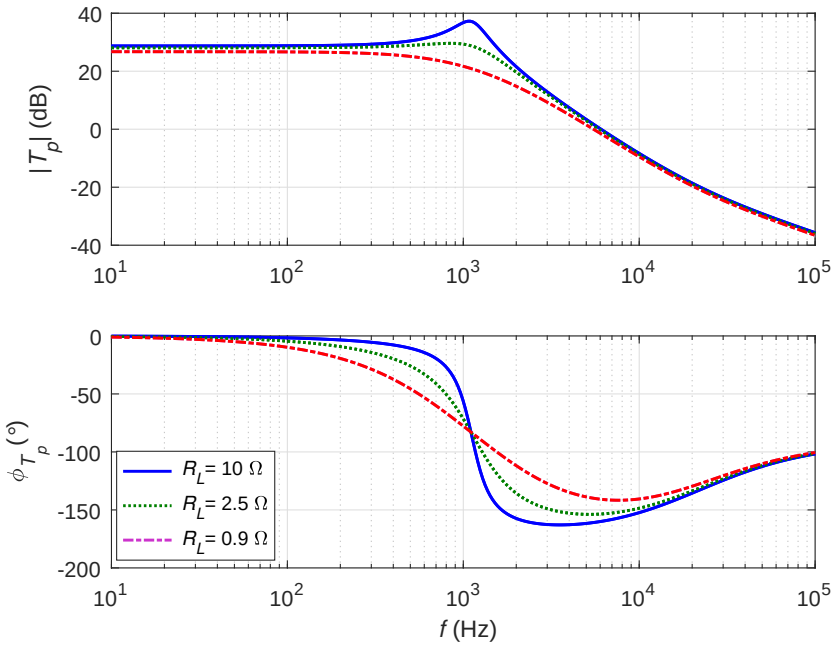

Figure 5.75: Bode magnitude and phase plots of T_p at selected values of R_L.

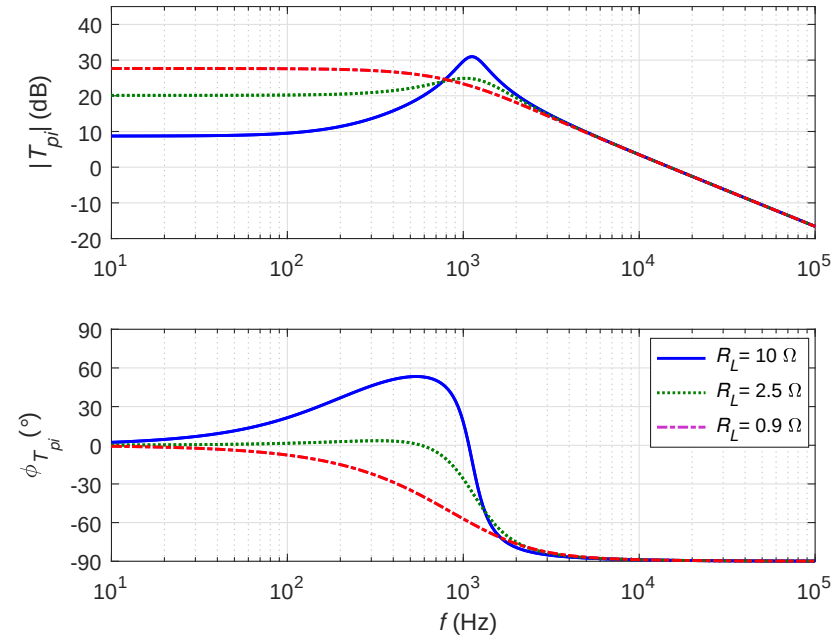

Figure 5.76: Bode magnitude and phase plots of T_{pi} at selected values of R_L.

6 Conclusions

6.1 Summary

The following topics have been covered in this dissertation:

1. Case study was performed on buck-boost dc-dc power converter.
2. Implementation of the proposed "True-Average" current-mode control technique, which can potentially overcome the problems in the existing techniques.
3. Analysis of the steady-state waveforms and design of the inner-current loop.
4. Development of small-signal models using circuit-averaging technique and block diagrams relevant to the inner-current loop.
5. Derivations of control and disturbance transfer functions related to closed-inner loop.
6. Evaluation of ac and transient characteristics.
7. Model verification through simulations.
8. Experimental validation of inner-current loop of buck-boost converter.
9. Development of block diagrams with closed-outer loop in the presence of inner-current loop.
10. Derivations of control and disturbance transfer functions for the two-loop system.
11. Evaluation of ac and transient characteristics for the two-loop system.
12. Model verification through simulations for the two-loop system.
13. Experimental validation for closed-loop buck-boost converter with ACMC.

14. Implementation of the proposed technique on buck converter and boost converter and verification with simulations.

6.2 Conclusions

The main conclusions of this dissertation are:

1. The subharmonic instability at low duty cycles is mitigated in the proposed control scheme.

2. The true-average current-mode control can accurately, sense, track, and regulate only the average inductor current.

3. Current in any branch in the converter, irrespective of the magnitude of the ripple can be sensed and controlled.

4. The control circuit and the filter circuit can be designed independently.

5. The RHP zero of the power-stage is not relocated by the inner current loop. Only the complex-conjugate poles of the power-stage are relocated and moved to a higher frequency. As a result, the bandwidth of the current-loop is wider than the power stage. Note that, in single-loop voltage-mode control, the RHP zero reduces the overall bandwidth with negative feedback and is a major drawback of voltage-mode control.

6. The inner current loop compensates the outer loop by providing a significant phase boost around the RHP zero frequency.

7. The outer loop in the presence of the inner loop provide nearly 100% correction to step change in supply voltage and the load.

8. The current loop bandwidth is nearly 3 times higher than the open-loop bandwidth at any duty cycle and load.

9. Noise and other undesirable interference are generated by the logic circuits in peak current-mode control. Whereas, average current-mode control is immune to noise, thereby improving the quality of control signals.

10. Basic voltage-mode control has the following disadvantages:

    - Slow response (or low bandwidth) due to large filter capacitor.
    - Presence of RHP zero in non-minimum phase converters (boost and buck-boost) require stronger controller such as Type-III or double-lead compensators.
    - Stability issues, when consecutively cascaded due to slow regulation.

    The above problems are mitigated by average current-mode control. The inner-current loop combined with the power-stage creates a much friendlier plant for the voltage loop, which improves the overall dynamic performance significantly.

6.3 Future Work

The future works includes:

1. Implementation of the proposed true-average current-mode control technique to other converter counterparts such as Ćuk, SEPIC, dual-SEPIC, half-bridge, full-bridge, and push-pull converters.

2. Detailed study of the dynamic performance in the presence of high-order compensation schemes such as Type III and implementation of the same using digital control schemes.

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